Impact Factor (SJIF): 4.542

International Journal of Advance Research in Engineering, Science & Technology

e-ISSN: 2393-9877, p-ISSN: 2394-2444

Volume 4, Issue 3, March-2017

2.4 Gbps CLOCK AND DATA RECOVERY USING CMOS 45nm TECHNOLOGY

Hiren B. Ravisaheb [1], Bharat H. Nagpara [2]

[1]*P.G. Student, Dept. of EC, C. U. Shah College of Engineering & Technology, Wadhwancity ,Gujarat*
[2]*Asst. Prof. , Dept. of EC, C. U. Shah College of Engineering & Technology, Wadhwancity, Gujarat.*

Abstract — The bandwidth demands of modern computing systems have been continually increasing and the recent focus on parallel processing will only increase the demands placed on data communication circuits. As data rates enter the 2.4Gb/s range, serial data communication architectures become attractive as compared to parallel architectures. Serial architectures have long been used in fiber optic systems for long-haul applications, The integration of clock and data recovery circuits into monolithic integrated circuits is attractive as it improves performance and reduces the system cost, The functionality and implementation of these circuits will be checked in LTspice using standard 45nm CMOS technology.

Keywords- Phase Frequency Detector, Charge Pump, Low Pass Filter, Voltage Controlled Oscillator, Retimed Data Circuit, LT Spice Tool.

I. INTRODUCTION

The exponential growth experienced by the global communication networks has resulted in a demand for increasingly faster communication systems, capable of rapidly processing and transmitting all generated data.The transmission of these data is nowadays realised by means of optical fiber channels because they achieve the best bandwidth and loss performance. However, the stages attached to the emitting and receiving ends typically use electrical signals to operate.

As a consequence, there is a need to design conversion circuits from optical to electrical signal and vice-versa. These systems have to be fast enough for the whole network to fully take advantage of the excellent properties that optical fiber channels present.At the receiving end of a typical optical communications system, the conversion and conditioning from optical to electrical signal is realised by a succession of stages. One of the most critical stages of this process is the clock and data recovery circuit (CDR), whose mission is the extraction of a clock signal from the incoming data, the synchronisation of both signals and the regeneration of the incoming data stream.

Typically, a CDR is formed by a phase detector (PD), a charge pump (CP) and loop filter (LF), Low pass Filter, a voltage controlled oscillator (VCO), and a Retimed Data Circuit. Fig1 shows the Block Diagram of clock and data recovery circuit.

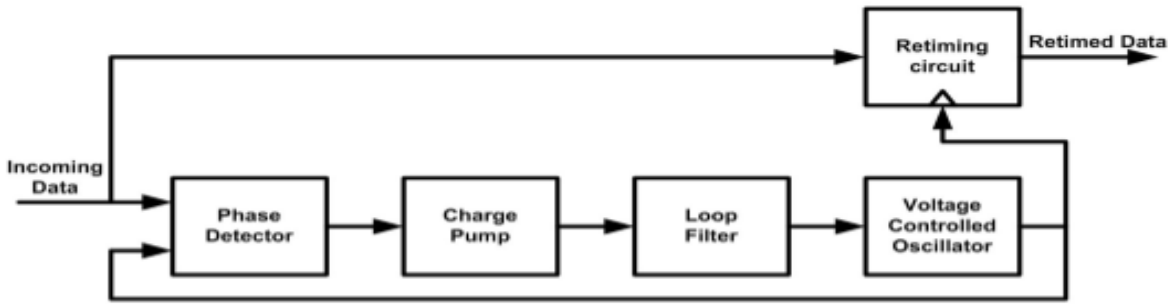


Fig.1 Block Diagram of Clock and Data Recovery

II. SYSTEM ARCHITECTURE

The function of a CDR circuit is to receive a serial data stream, synchronize an internal clock to the data signal, and then use that clock to retime the data. The output of a CDR circuit is logically identical to the input signal, however the signal-to-noise ratio (SNR) of the output signal is increased. It is possible to build CDR circuits with either open-loop or closed loop architectures, however closed loop architectures dominate in monolithic implementations. One significant problem with open-loop CDR circuits is that they generally require the use of high Q filters, which cannot be integrated

into a CMOS environment. The closed-loop CDR architecture is often referred to as a phase-locking CDR circuit, and its architecture is similar to that of the phase-locked loop (PLL) circuit.

The closed-loop CDR circuit is much easier to integrate than the open-loop CDR circuit, and as such in this thesis any reference to a CDR circuit implies the phase-locking CDR circuit topology. The architecture of a PLL based CDR circuit is given in Fig.1 . The phase detector detects phase errors between the incoming data signal and the internal clock signal and supplies correction information to the charge pump. The charge pump takes the correction information and adds charge to or subtracts charge from the loop filter.

The loop filter plays an important role in defining the frequency response of the system. The voltage on the loop filter controls the VCO, and the output of the VCO is sent to both the phase detector and also to the retiming circuit. Here, There are two types of circuit used

1. PLL
2. Retimed Data Recovery Circuit

PLL is used for recovering clock and retimed data circuit is used for recovering the data

Let's explain all the component of CDR in details.

2.1 Phase Detector

There are two types of Phase Detector used in PLL.

1. XOR Phase Detector
2. Phase Frequency Detector

In CDR , We are used AND gate based PFD.

It consists of two edge triggered D flip flops with their D inputs tied to logic 1 and a AND Gate in the reset path. In reset path NAND, NOR gate can be used. PFD compare Ref signal and Div signal. Generate three sequential logic states for controlling Charge Pump. Fig.2 shows the PFD using AND gate.

The circuit consists of two edge triggered D flip flops DFF which is resettable, with their D inputs tied to logic 1 and a AND Gate in the reset path. The Ref and Div serve as clocks of the flip flops. Suppose the rising edge of Ref leads that of Div, then UP goes to logic high. UP keeps high until a low to high transition occurs on Div. Because UP and DN, are AND, so Reset goes to logic high and resets the PFD into the initial state.

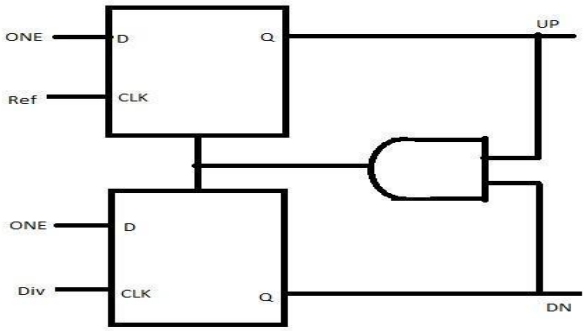


Fig.2 AND gate based PFD

The PFD is a state machine with three states. When Ref leads Div, the UP output is asserted on the rising edge of Ref. and UP signal goes high.

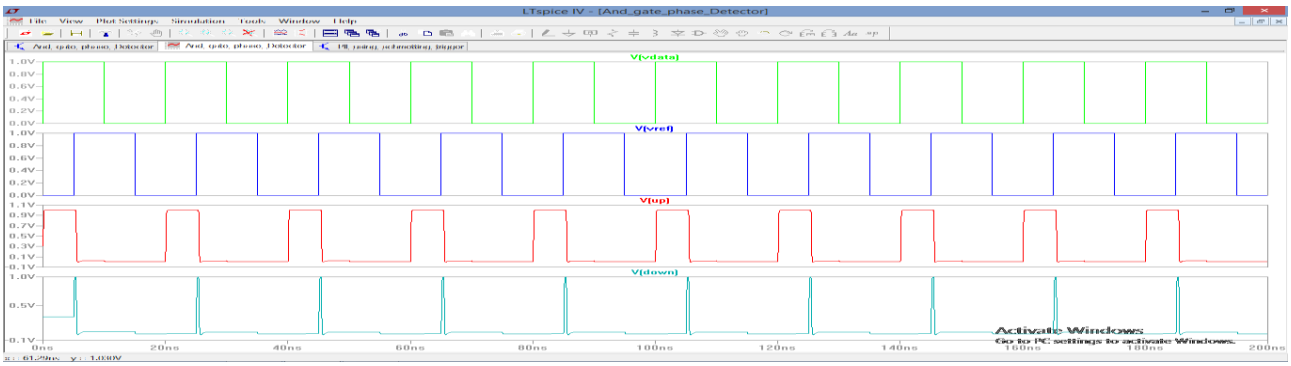


Fig.3 (a) when data signal leads the clock signal

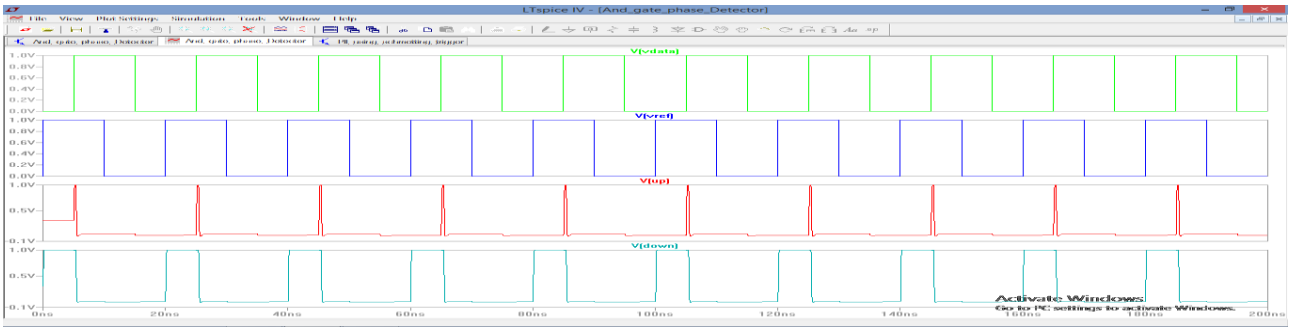


Fig.3 (b) When clock signal leads the data signal

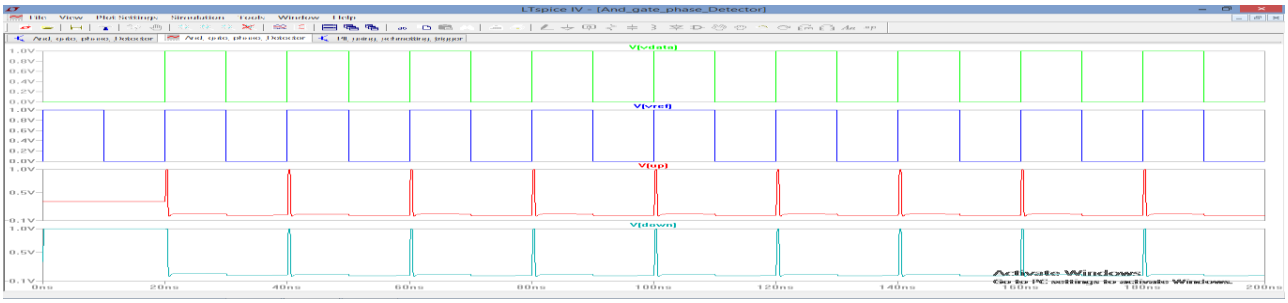


Fig.3 (c) when clock and data signal are same

2.2 Charge Pump

A charge pump is three state designs. It takes two inputs out from the PFD and outputs a DC current or voltage. The charge pump consists of two current sources and the output of the charge pump drives the low pass filter. The charge pump either charges or discharges a capacitor with voltage or current pulses. A filter is used to limit the rate of change of the capacitor voltage, and the result is a slowly rising or falling voltage that depends on the frequency difference between the PLL output voltage and the reference frequency. The VCO increases or decreases its frequency of operation as the control voltage is increased or decreased. Following figure 4 shows the charge pump.

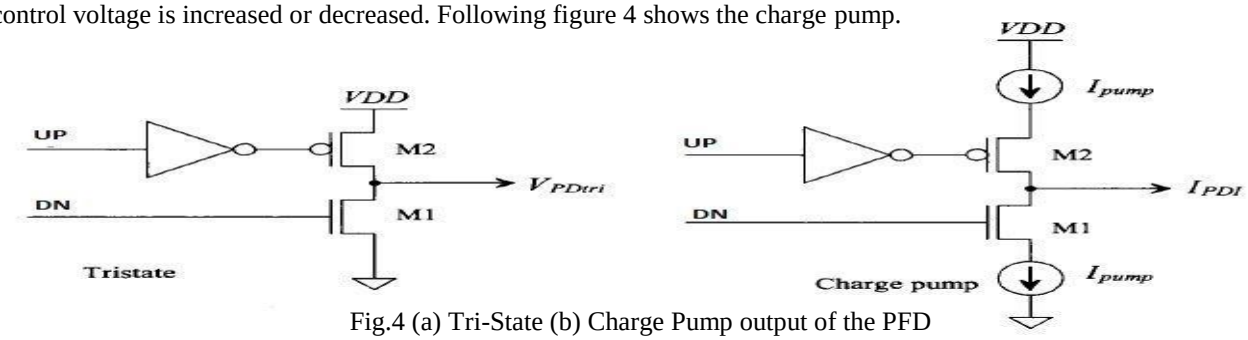


Fig.4 (a) Tri-State (b) Charge Pump output of the PFD

2.3 LOOP FILTER

The design of the loop filter is the principle tool in selecting the bandwidth of the PLL. A PLL without a loop filter result in a 1st order system. First order system is rarely used as they offer little noise suppression. Since higher order loop filters offer better noise cancelation, loop filters of order 2 and more are used in critical applications, such as in the case of clock and data recovery. The purpose loop filter is to convert the charge pump current Icp into a voltage controlled signal Vctrl, to filter the alternating current component and to suppress the noise.

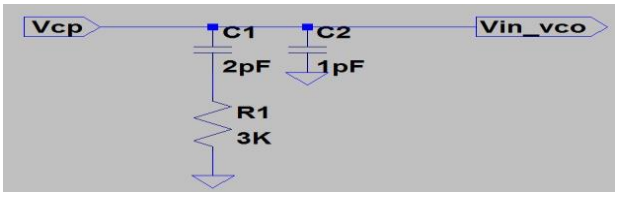


Fig.5 Loop Filter

2.4 CURRENT STARVED VCO

VCO is a frequency modulated oscillator whose instantaneous output frequency is directly proportional to its control voltage. A ring oscillator can be smoothly integrated in a standard CMOS process without taking extra processing steps because it does not require any passive resonant element compare to CMOS LC-tank oscillator. In this work 5-stage CMOS inverter forms a closed path with positive feedback . The schematic of the whole VCO is shown in fig 1.Voltage control oscillator have a CMOS inverter circuit as shown in figure6.This inverter circuit is connected to current sources M3 and M4 that limit the current available to the inverter. The currents in MOSFETs M1 and M2 are mirrored in each inverter stage.

The oscillation frequency of the current-starved VCO for N (an odd number > 5) of stages is

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{N \cdot C_{tot} \cdot VDD}$$

Which is f_center (@VinVCO = VDD/2 and ID = IDcenter) Schematic of current starved VCO is shown in figure6.with 5 stage

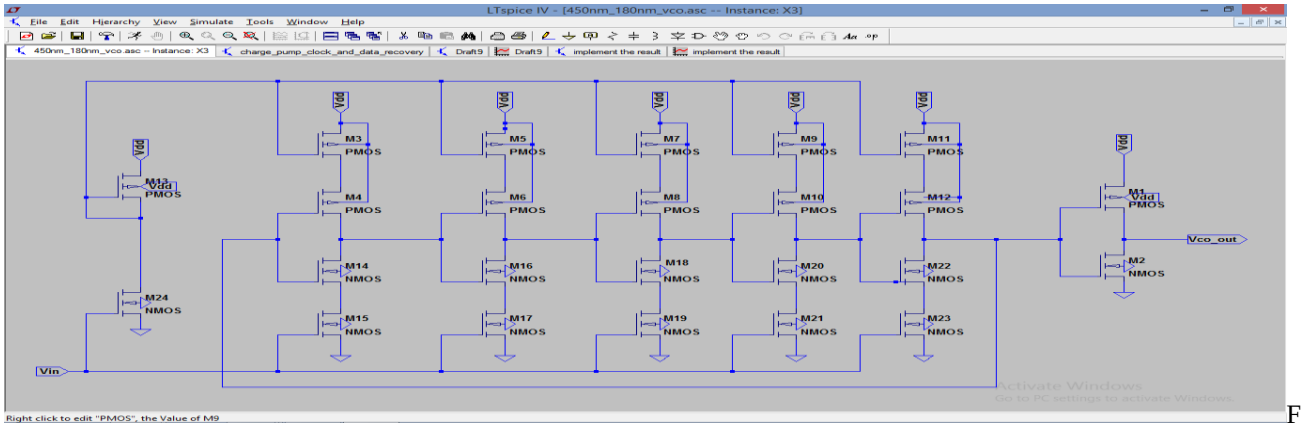


Fig.6 Current Starved VCO

Simulation Result of Current Starved VCO

The transient analysis of current starved VCO is shown in figure 6.1.For input control voltage, Vinvco, equal to 0.50mV, an output frequency of 1.2GHz has been obtained. The input control voltage is varied from 0.1V to 1V, in steps of 0.5V and output Frequency is observed.

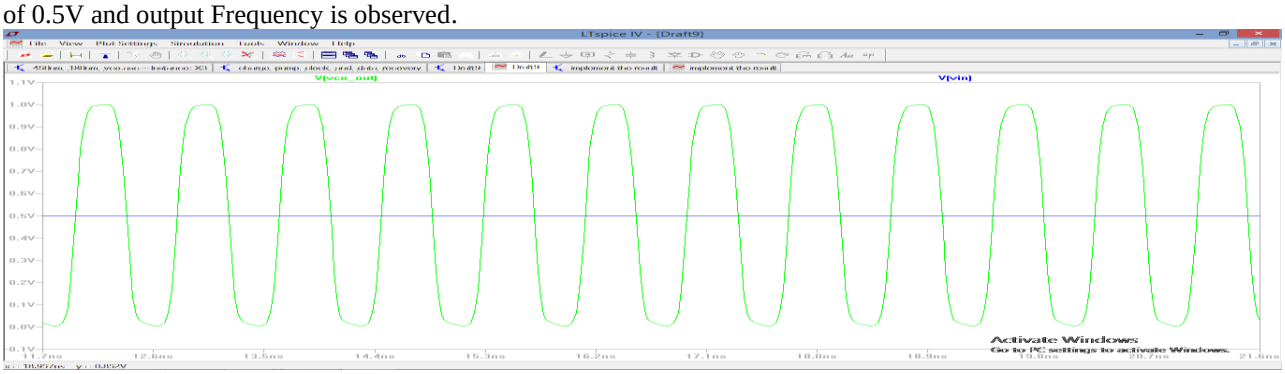
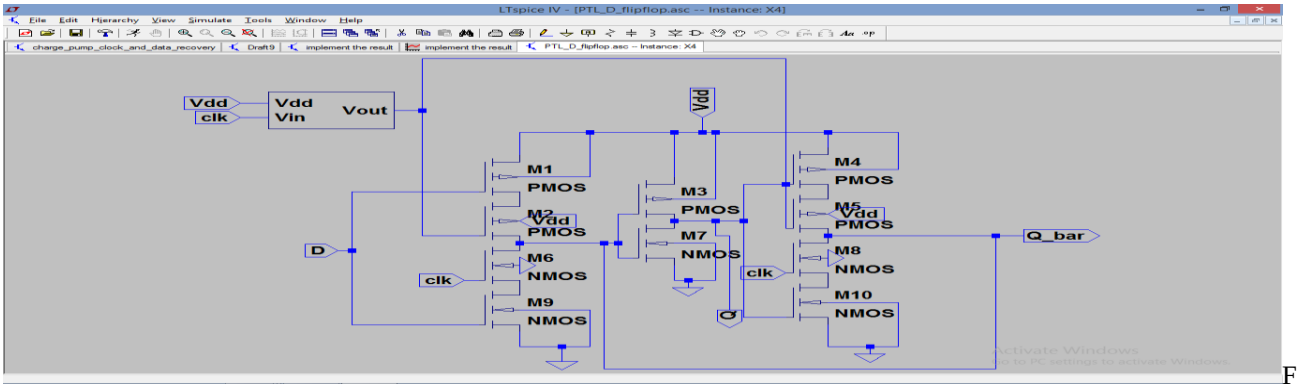


Figure 6.1 Waveform of VCO

2.5 RETIMED DATA RECOVERY CIRCUIT

In the Retimed data recovery circuit, there are two types of D Flip-Flop used. First one D Flip-Flop is used of regenerating the clock and secone one D Flip-Flop is used for recovering the data.

Here, First D Flip-Flop is PTL base , second D Flip- Flop is TSPC_18T



F

Fig.7(a) PTL Base D Flip-Flop

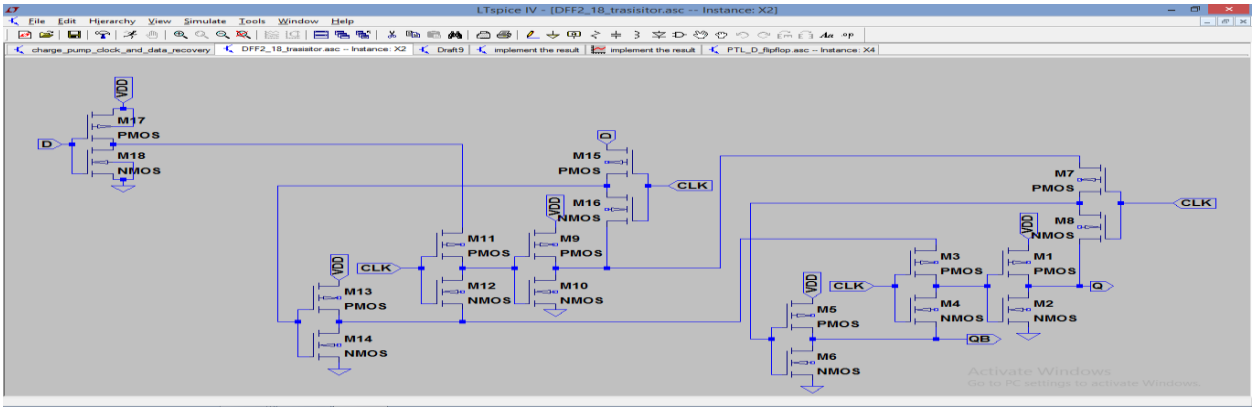


Fig.7 (b) TSPC_18T Base D Flip-Flop

Fig.7 (c) Show that output of the D Flip-Flop is delay clock which we applied the input of the clock signal

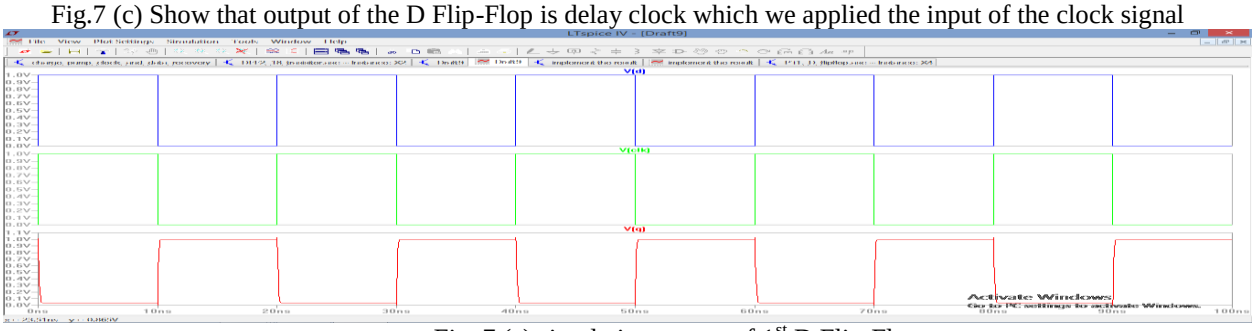


Fig. 7 (c) simulation output of 1st D Flip-Flop

Fig. 8 (b) shows that output of the D Flip-Flop is delay of the data which we applied the input of the data

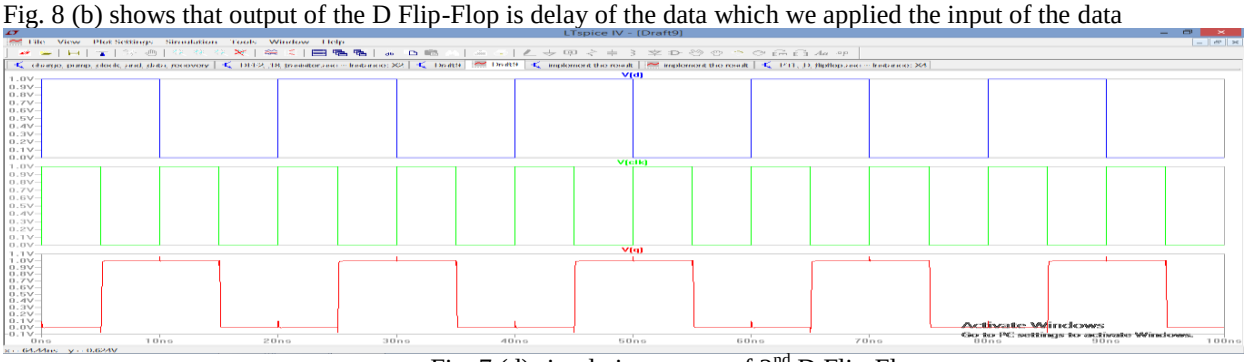


Fig. 7 (d) simulation output of 2nd D Flip-Flop

III. SIMULATION RESULTS

The clock and data recovery has been simulated by using 45nm CMOS technology. The complete CDR draws 0.368mW from a 1V voltage supply. Fig. 8(a)shows that When data 1100 is coming from the outside, we can get the correct data of output of second D flip-flop and recover the clock by PLL which frequency is 1.2 GHz.

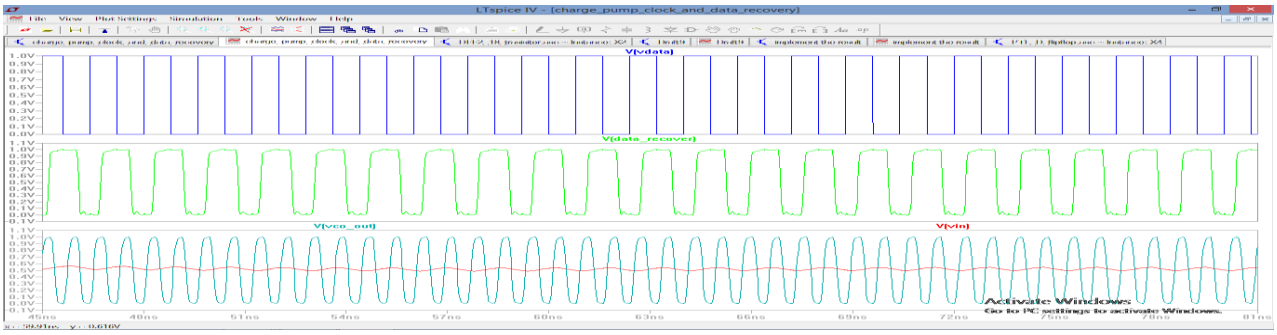


Fig 8 (a) 1100 data recovered by D Flip-Flop and clock recovered by PLL

Fig. 8(b)shows that When data 1000 is coming from the outside, we can get the correct data of output of second D flip-flop and recover the clock by PLL which the frequency is 1.2 GHz.

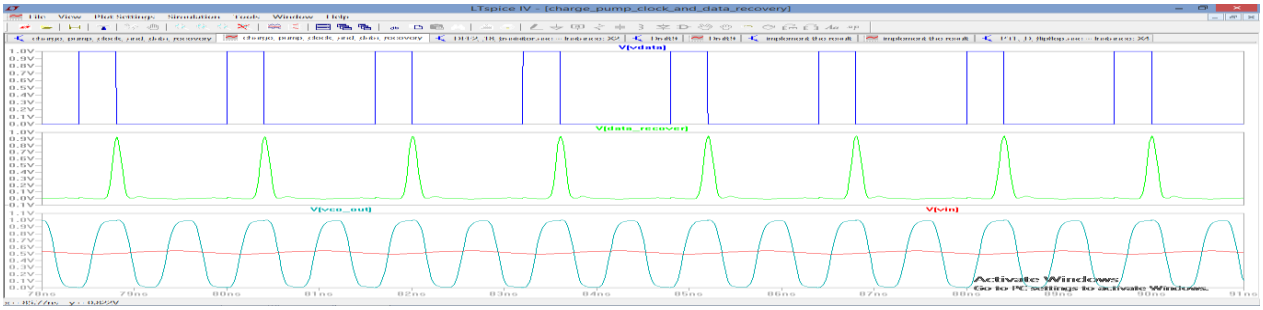


Fig 8 (b) 1000 data recoverd by D Flip-Flop and clock recovered by PLL

Fig. 8(c)shows that When data 1110 is coming from the outside, we can get the correct data of output of second D flip-flop and recover the clock by PLL which the frequency is 1.2 GHz.

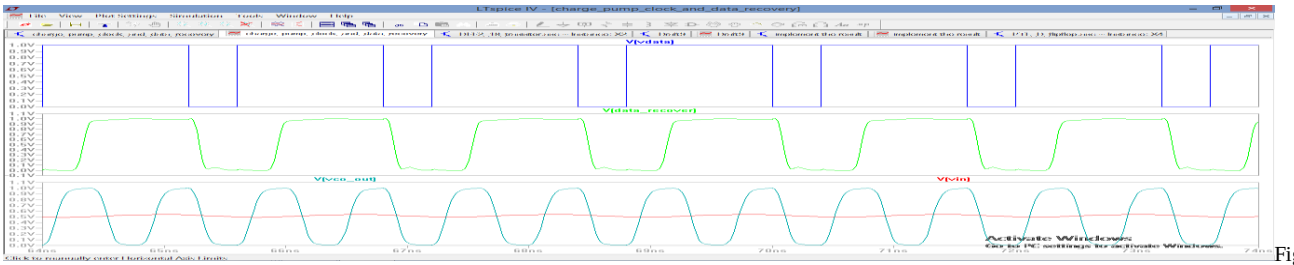


Fig.8 (b) 0001 data recoverd by D Flip-Flop and clock recovered by PLL

IV. CONCLUSION AND FUTURE WORK

A fully integrated clock and data recovery has been presented for wireless application. The design has been simulated 45nm CMOS technology. The VCO generates a center frequency at 1.24GHz at Vinvco of 0.53V approximately. The PLL settles in approximately 42ns, generates frequencies from 1.24 to 1.26 GHz . The measured phase noise is -48.32 dBc/Hz at 5 MHz offset and the power consumption is 0.368 mW. In future we can design multi level phase detector using cmos technology and by using this multi level phase detector we design the clock and data recovery circuit.

Table I

Parameters	**Result of current work**
Technology	45nm
Supply voltage	1V
Frequency Rang	1.24 – 1.25 GHz
Lock Time	50ns
Phase Noise	-48.32dBc/Hz at 5 MHz offset
Power Dissipation	368.186 uW
Data Recover delay time	412.31 ps

REFERENCES

[1] Taek-Joon An, Jin-Ku Kang Department of Electronics Engineering Inha University 978-1-4799-1122-4/13 2013 IEEE "A 5-Gb/s 11.4mW Half-Rate CDR in 0.18—m CMOS"

[2] T.Thangam , P. Jeya Priyanka, V.Sangeetha ,International Journal of Electronics Signals and Systems (IJESS) ISSN 2348 – 7968, Vol. 2 Issue 4, April 2015," Performance Improved Low Power D-Flip Flop with Pass Transistor Design and its Comparative Study".

[3] Chih-Lin Chen, Student Member, IEEE, and Chua-Chin Wang†, Senior Member, IEEE2011 IEEE "A Fast-locking Clock and Data Recovery Circuit with A Lock Detector Loop"

[4] C. Sanchez-Azqueta, S. Celma, European confereance on circuit theory and design IEEE 2011, "A Phase Detection Scheme for Clock and Data Recovery Applications"

[5] Do Jeong, and Hang-Geun Jeong, International Journal of Electrical, Electronic Science and Engineering Vol:1 No:7, 2007 "A 3.125Gb/s Clock and Data Recovery Circuit Using 1/4-Rate Technique "

[6] Chung Hwan Son and Sangjin Byun, Member, IEEE, April 7, 2016 "On Frequency Detection Capability of Full-rate Linear and Binary Phase Detectors"

[7] Kisang Jung, Kangjik Kim, Chimin Park, Sanghoon Jeong, Seongik Cho, Recent Advance in Circuits, System, Signal and Telecommunications ISSN: 1790-5117"Clock and Date Recovery Circuit Using 1/4-rate Phase Picking Detector"

[8] Sangjin Byun, Member, IEEE, 1549-8328 © 2016 IEEE "A 400 Mb/s~2.5 Gb/s Referenceless CDR IC Using Intrinsic Frequency Detection Capability of Half-Rate Linear Phase Detector"