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FPGA Based Design and Implementation of Ternary Content Addressable Memory(TCAM) Using Reversible Logic gates.

Manjunath C Bajantri,

Student

Department of VLSI and Embedded Systems

Center of P G Studies VTU Belagavi.

Mr Mahesh Neelagar

Asistant professor

Department Of VLSI and Embedded Systems

Center of P G Studies VTU Belagavi.

Abstract--- CAM is the one of the special type of memory Which is used to search the contents stored in the memory using the contents. Ternary content addressable memory is a memory which has three states logic 1,logic0 and logic x where search operation is performed within the single clock cycle. This memory component is designed using the reversible logic gates .

Keywords- Ternary Content addressable memory(TCAM),Selection line, Match Line, Word line, Match Bit

RAM(Random Acess Memory).

I. INTRODUCTION

Ternary content Addressable memory is a one of the Special type of memory ,these memory has the three logic states ie: Logic “0”, Logic “1” and Logic” x” this is used to perform the search operation within the Single Clock Cycle. TCAM finds the application in various field. The main application of TCAM is found in the Network Routers where searching operation is done using the Contents . The other applications of the TCAM are found in Intrusion Detect, image processing, Gene pattern searching bioinformatics. The proposed concept is designed using the reversible logic gate . In Reversible logic gates, each and every computed information is stored, because of that there is no loss of data and loss of power. There are equal number of inputs and outputs in reversible gates and the information is reused in the circuit by avoiding the loss of information by not computing the information computed before. There are three factors in the reversible logic ,Quantum cost ,Worst case Delay and Garbage outputs. There are few gates proposed namely Toffoli Gate which has the quantum cost of 5 which has 3 inputs and 3 outputs and Feyman gate has quantum cost of 1 and has two inputs and two outputs similarly many reversible gates have been proposed satisfying all the reversible properties.

II LITERATURE SURVEY

More research is done on the reversible logic gates. The processing of the reversible logic gates is a basic method of reusing[1].Using the TR gate a binary subtractor is proposed , TR gates stands better then that of the other reversible gates available and by using this reversible logic gate the garbage output ,quantum cost and circuit complexity is reduced .TCAM is used in many High speed searching applications one of the well known application is Internet Router, where CAM or TCAM is used to search the content of the memory and gives out the Address of respective memory to the RAM[2].There are many applications of reversible logic gates in Low Power CMOS which are used in CODE Converters, Bioinformatics which are designed by utilizing the Basic available Reversible logic gates . Converters reduce the switching activities by pointing the transition between single and many ordered logical operations[3].

Cam Compares the stored bits with the search line bit which is fed from the input side and there are two types of CAM ie Binary CAM and Ternary CAM. Binary CAM has only Two states “logic 0” and logic”1” and in Ternary CAM there are Three states Logic “1” ,Logic “0” and Don’t Care , Hashing technique is used in CAM Based RAMS which is nothing but the conversion of long data into the short Key .

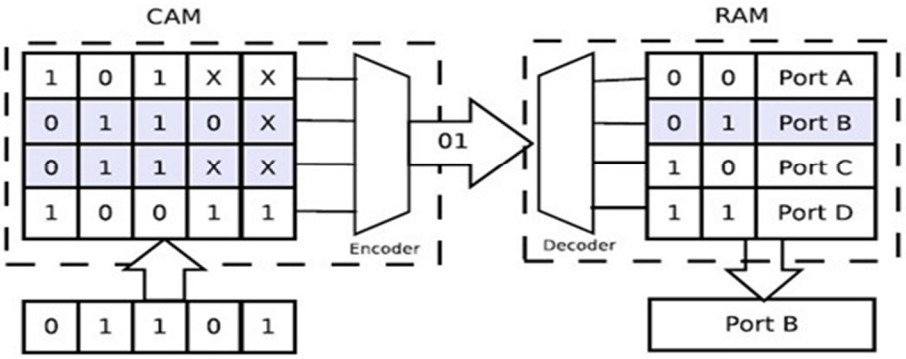

Figure 1: Basic operation of TCAM

III Basic Reversible Logic Gates and Operation

Reversible Logic gates are nothing but the gates having the same number of inputs as well as same number of outputs. Where the inputs and outputs of the gate are mapped with each other. There are 3 factors related to the reversible logic gates ,Quantum cost, Worst case delay and garbage outputs.

Feyman gate which is said to be controlled Not gate having two inputs and two outputs which is said to be 2x2 and having the quantum cost of 1with worst case delay of 1. Fredkin gate is 3x3 reversible gate having the quantum cost of 5 and worst case delay of 5. Tofoli gate is 3x3 one of the reversible gate having the quantum cost of 6 with worst case delay of 6.peres gate is also 3x3 the member of reversible logic gate family with quantum cost of 4 with worst case delay of 4.

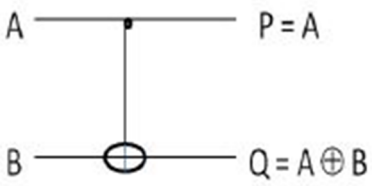

Figure 2: Feyman gate

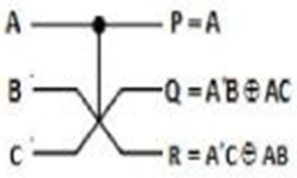

Figure 3:Fredkin gate

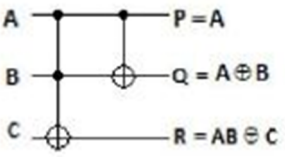

Figure 4: Peres gate

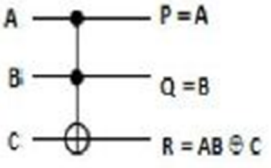

Figure 5: Tofoli gate

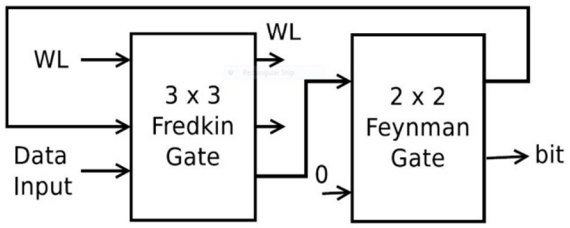

Figure 6: Reversible SRAM

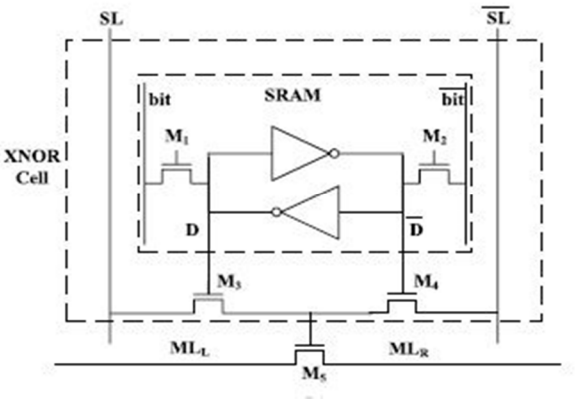

Figure 7: Conventional TCAM

IV. Working of SRAM and TCAM

In this section we are going to discuss about the SRAM using reversible logic gates and about the conventional TCAM realized using the Conventional logic gates. Figure 6 shows the realization of the SRAM using reversible logic gates . Here in proposed design we use 3x3 Fredkin gate and 2x2 Feyman gate to realize the SRAM. This SRAM has the capacity to store single bit of data in it. SRAM has two states Hold state and Read/Write State . The operating modes of the SRAM Depends upon the WL when WL=0 SRAM operates in Hold State and When WL=1 SRAM operates in Read/ Write Mode . Figure 7 shows the Diagram of Conventional TCAM . it consists of Two back inverted inverters connected to each other in opposite direction which acts as a memory to store a data it consists of SL and SL_bar which are known as search lines which are used to search the bit stored in the memory and ML(match line) which is output of the TCAM.

V. Working of Reversible TCAM

In this part we discuss about the Single bit TCAM Realized Using the Reversible Logic gates . The Input data is given from the SRAM to the TCAM cell as a input to Feyman gate which is then connected to Feyman gate and then connected to the Fredkin gate the exored results is given as input to the to peres gate where output is obtained at Match line(ML) the same TCAM can be Realized by replacing the Peres gate by Tofoli gate .But the quantum costof the Second design increases slightly which also effects the worst case delay of the circuit also but garbage outputs remain same for the both the design.

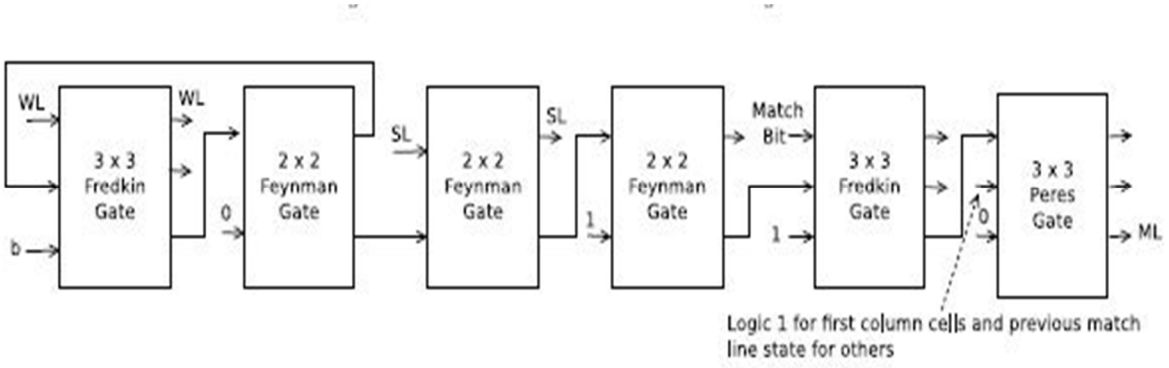

Figure 9: Reversible TCAM Using Reversible Logic gates

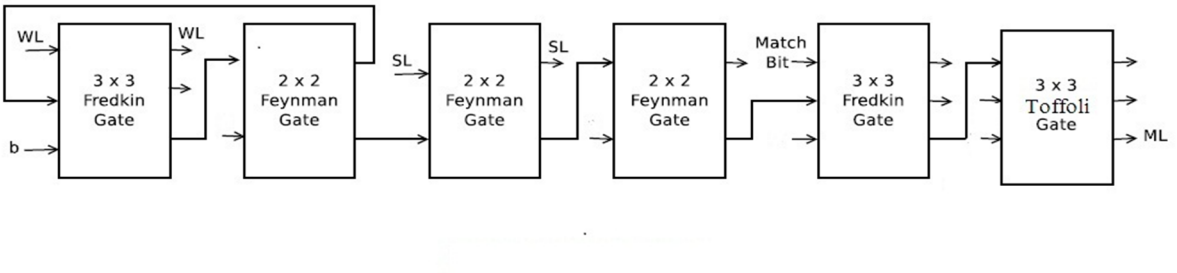

Figure 10: Reversible TCAM using Tofoli Gate

VI. Results And Discussion

In this part we Discuss the Simulated Results of the Above Design and Verified it Using Xilinx ISE Simulator 14.7 on Spartan 6 Board

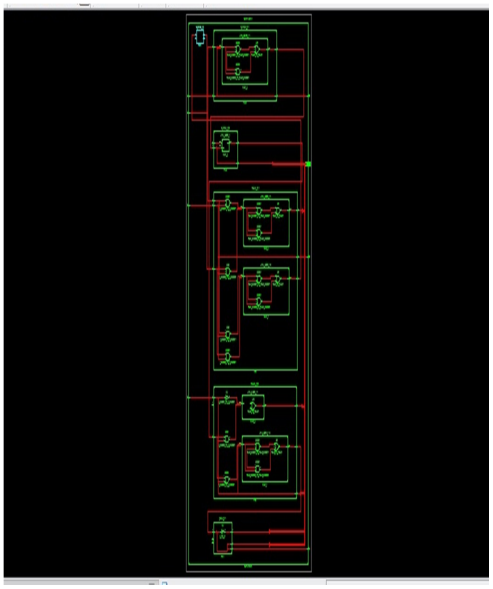

Figure 12: RTL for TCAM using peres gate

Figure 13: RTLfor TCAM using Tofoli gate

Comparisons Of Both the Designs

Model	Quantum cost	Worst case delay	Garbage Output
Single bit TCAM with Toffoli gate	18	18	6
Single bit TCAM with Peres gate	17	17	6

VII. Conclusion and Future Scope

Above two Designs perform the same operations which are verified on Xilinx ISE 14.7 simulator and compared the designs interms of cost performance and garbage Outputs which varies slightly In above designs we have only tried to reduce the quantum cost and delay of the circuitand compare the both the design for single bit we can also design for array of cells and compare the results which is also done using Xilinx tool and verified on FPGA kit.

VIII. Refrences

[1] Sk Noor Mahammad, Siva Kumar Sastry Hari,, " Constructing Online Testable Circuits Using Reversible Logic Reconfigurable and Intelligent Systems Engineering Group.

[2] Kostas Pagiamtzis , Ali Sheikholeslami, "Content-Addressable Memory (CAM) Circuits and Architectures: A Tutorial and Survey", *IEEE JOURNAL OF SOLID-STATE CIRCUITS VOL. 41, NO. 3, MARCH 2006*

[3] Vinay Kumar Gollapalli and K Koteshwarrao, M. Tech, SSGN Srinivas, M. Tech, "Design of Reversible Code Converters Using Verilog HDL",International journal and Magazine of Engineering technology management and Research, 2015.

[4] Md. Selim Al Mamun, David Menville " Quantum Cost Optimization for Reversible Sequential Circuit" *(IJACSA) International Journal of Advanced Computer Science and Applications, Vol. 4, No. 12, 2013*.

[5] Jagadeesh. D. Pujari, Rajesh. Yakkundimath and A. S. Byadgi, "Algorithm andArchitecture for a Low-Power Content-Addressable Memory Basedon Sparse Clustered Networks ", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 23, NO. 4, APRIL 2015.

[6] Matthew Morrison, Matthew Lewandowski, Richard Meana, "Design of Static and Dynamic RAM Arrays using a Novel Reversible Logic Gate and Decoder", 2011 11th IEEE International Conference on Nanotechnology Portland Marriott August 15-18, 2011, Portland, Oregon, USA

[7] S Dinesh Kumar Noor Mahammad Sk, "A Novel Ternary Content-Addressable Memory (TCAM) Design Using Reversible Logic", 2015 28th International Conference on VLSI Design and 2015 14th International Conference on Embedded Systems .

[8] Md. Selim Al Mamun, Pronab Kumar Mondal,Uzzal Kumar Prodhan," A Novel Approach for Designing Online Testable Reversible Circuits" International Journal of Engineering Research and Development **e**-ISSN: 2278-067X, **p**-ISSN : 2278-800X, www.ijerd.com Volume 5, Issue 2 (December 2012), PP. 39-44.

[9] B.Raghu kanth*, B.Murali Krishna "A DISTINGUISH BETWEEN REVERSIBLE AND CONVENTIONAL LOGIC GATES" International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 2,Mar-Apr 2012, pp.148