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Analysis of Positive Output Super Lift Luo converter with discrete time controller for Digital Applications

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Abstract: -- This paper presents an Observer based approach to improve the dynamic responses of the positive output super lift Luo converter controlled by a digital controller. The dynamics of the closed loop system is investigated using discrete time modeling technique which includes the dynamic compensation in the form of prediction observer controller for obtaining output variable regulation. The discrete model for the entire system is used to predict the instability of the converter system for line and load disturbances. The implementation which includes the digital state feedback and a load estimator is very simple and well suited for the digitally controlled PWM converters. It has been investigated by choosing an appropriate feedback matrix and load estimator to eliminate the error and to estimate the immeasurable state variables in order to obtain zero output voltage error, stability, robustness and stiff output voltage regulation. The feasibility and functionality of the proposed system is verified using simulation and experimental prototype of digitally controlled PWM Positive Output Super Lift Luo converter.

I. INTRODUCTION

In the past few decades, digital control of PWM dc-dc power converters has been widely carried out and investigated by the researchers due to the several salient features such as low sensitivity to disturbances and disparity in resonant components, simplicity to assimilate with other digital structures, capability to realize sophisticated control methods and possibility to modernize controllers by using software [1].Power Electronics is the vast field which mainly places a challenge on controlling the non linear dynamics of the wide varieties of dc-dc converter topologies. One amongst the recent advancement in converter family is LUO converters. LUO converters are the simplest converters derived from Buck-Boost converters used for step up/step down operation with high power density and high power efficiency.

With the advent of new technique like voltage lift technique, several researches are being carried out in implementing this method in the dc-dc converters which in turn paves the way to design high gain converters. Voltage lift technique efficiently improves the voltage gain transfer in power converters and the converters like Positive output super lift Luo(POSLL) converters in which this technique can be employed are widely used in many applications such as in computer peripheral equipments and industrial applications [2].

The performance of the switching mode regulators are mainly influenced by the control techniques. The current mode control technique overrides the conventional voltage mode control in recent years due to several advantages such as, higher loop bandwidth gain, faster response, inherent over current protection and improved input transient response. However the systems with current mode control become unreliable and cost effective since it requires an additional module for the inductor current sensing. Hence it is entailed to implement a sensor less current controlled dc-dc converter which requires no additional current detecting device or voltage level shifting devices to meet out the aforesaid advantages**.**

In this paper, an effort is made to investigate the performance of the sensor less digital current mode control of Positive output super lift Luo converter. Since the state space averaging technique is a simpler and the most widely used method for modeling, the POSLL converter is modeled using this method. The performance analysis of the POSLL converter is done by operating the converter in continuous conduction mode. The sections are organized as follows: Section 2 consists of overall block diagram, sections 3 & 4 consist of system description and modeling of POSLL

converter, section 4 consists of the design of discrete controller design and analysis, sections 5, 6 & 7 consist of simulation results and discussion, hardware results and conclusion respectively and the references are given at the end.

II. DISCRETE CONTROLLER AS A CLOSED LOOP

The closed loop system of POSLL converter is described in the following figure 1.

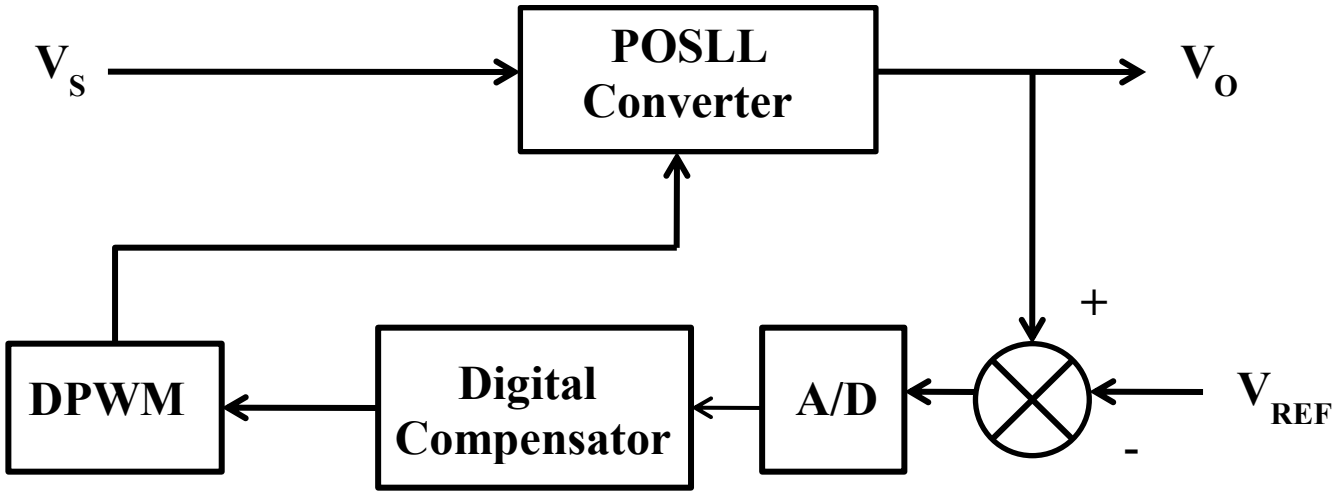

Fig.1 digitally controlled POSLL converter employing Observer

The ultimate objective is to provide a dynamic compensation for the POSLL converter using current mode controlled discrete Observer controller in continuous conduction mode. Here the Observer design is derived from the state space model of the converter so that the inductor current which is one of the state variables can be amalgamated from the measured variables like input and output voltages. In other words the unmeasurable state variables can be estimated since all the variables cannot be measured at all times. The closed loop system is a typical two loop system employing inner current loop and outer voltage loop. The outer voltage loop provides the reference current for the inner loop and thus the inductor current is controlled in order to obtain regulated output voltage. Controller design involves two steps. In the first step a digital control law is derived in order to obtain the stability of the converter where as in the second step a load estimator is designed which acts quickly on the error resulting in zero steady state output error.

III. SYSTEM DESCRIPTION

One of the most popular techniques mainly used for electronic circuit design is the voltage lift technique and in recent years this technique finds wider application in dc-dc power converters. One such type of a converter is the Positive output Super lift Luo converter and its schematic diagram is illustrated in Fig.2. Using voltage lift technique this type of converter converts positive voltages into positive voltages and the first quadrant operation is obtained with larger voltage amplification when compared with the basic Boost converters.

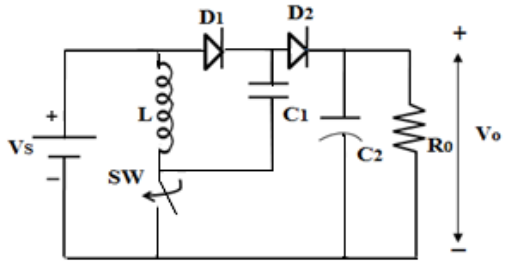

Fig.2 Schematic diagram of a POSLL Converter

In fig.2 V_S denotes the positive input dc voltage, V_O denotes the corresponding output voltage, SW denotes an n-channel MOSFET, D_1 and D_2 are the freewheeling diodes, L is the inductor and C_1, C_2 are the capacitors. In order to achieve high power density the converter is operated in continuous conduction mode with all the parameters assumed as ideal one.

There are two operating modes in POSLL converter which is explained as follows.
Mode1 corresponds to the ON time of the switch and mode 2 corresponds to the OFF time of the switch.
Mode1: When the switch is closed, the diode D_1 starts conducting and within a very short period of time the capacitor C1 begins to charge and accomplishes a constant voltage level of source voltage, V_S. The current flowing through the inductor depends on the input voltage. The capacitor C_2 supplies energy to the load R_O. Fig. 2 (a) illustrates the equivalent circuit of the POSLL Converter for mode 1 operation.

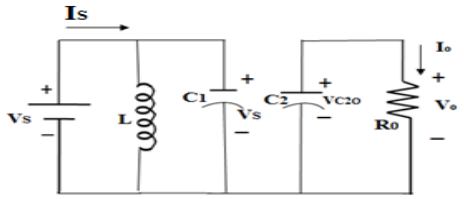

Fig. 2(a) Equivalent circuit of POSLL Converter for mode1

Mode 2: When the switch is opened, the diode D_2 conducts and the energy to the capacitor C_2 and the load resistance R_O are supplied by the diminishing value of inductor current. At the end of this mode, the inductor current decreases to a value of $(V_O - 2V_S)$. The equivalent circuit of POSLLC for this mode of operation is shown in fig. 2(b).

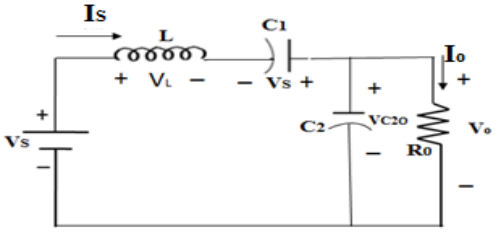

Fig. 2(b) Equivalent circuit of POSLL Converter for mode 2

Based on the above discussion the peak – peak ripple value of the inductor current and peak- peak ripple voltage of the capacitor is obtained as follows:

$$\Delta i_L = \frac{(V_O - 2V_S)}{L} T_{off} \qquad (1)$$

Where T_{off} is the off time of the converter given by (1-α) T, where α is the duty cycle ratio and T is the total time period given by $T = T_{on} + T_{off}$.'Δi_L' is the peak-peak value of the inductor current. It is a regular practice to assume Δi_L as 10% to 30% of the load current.

$$\Delta V_C = \frac{(1-\propto)V_0}{fRC_2} \quad (2)$$

Where V_O is the output voltage of the converter and f is the switching frequency.'$\Delta V_C'$ is the peak-peak ripple value of the capacitor voltage and it is assumed as 1% to 2% of the voltage across the load [3]. By using the above formulae the L and C values thus designed for the POSLL converter is illustrated in Table.1.For each mode of operation of the system, the dynamic equations describing the system functions are state affine and time invariant which is described by the following set of equations,

$$\left.\begin{aligned}\dot{x}(t) &= A_1x(t) + B_1V_S(t), sw = 1\\ \dot{x}(t) &= A_2x(t) + B_2V_S(t), sw = 0\end{aligned}\right\} \quad (3)$$

Here sw = 1 signifies the on state of the switch and sw = 0 signifies the off state of the switch. A_1, A_2, B_1 and B_2 are the coefficient matrices given by,

$$\left.\begin{aligned}A_1 &= \begin{bmatrix}0 & 0\\ 0 & \frac{-\alpha}{R_oC_2}\end{bmatrix}\\ A_2 &= \begin{bmatrix}0 & \frac{\alpha-1}{L}\\ \frac{1-\alpha}{C_2} & \frac{\alpha-1}{R_oC_2}\end{bmatrix}\\ B_1 &= \begin{bmatrix}\frac{\alpha}{L}\\ 0\end{bmatrix}, B_2 = \begin{bmatrix}\frac{2-2\alpha}{L}\\ 0\end{bmatrix}\end{aligned}\right\} \quad (4)$$

The output equation of the converter is represented as

$$,V_0(t) = [0 \quad 1]x(t) \quad (5)$$

The discrete time modeling of the converter is obtained by transforming the state model in to a sampled system by using the relation $t = kT_s$, where T_s is the sampling time and the corresponding equation is described as,

$$x(kT_S) = e^{AkT_S}x(0) + \int_0^{kT_S} e^{A(kT_S-\tau)}Bu(\tau)d\tau \quad (6)$$

where τ is a variable. With the analog coefficient matrices, discrete equivalent is obtained by means of the following associated equations,

$$\left.\begin{aligned}G &= e^{AT_S}\\ H &= \int_{\tau=0}^{T_S} e^{A\tau}d\tau B\\ C_d &= C\\ D_d &= D\end{aligned}\right\} \quad (7)$$

where *G*, *H*, C_d and D_d are the coefficient matrices for discrete systems. For discrete time signal, the POSLL converter dynamic equations are obtained as follows using the values stated in Table I ,

$$\left.\begin{aligned}G &= \begin{bmatrix}0.9998 & -0.0334\\ 0.0111 & 0.9990\end{bmatrix}\\ H &= \begin{bmatrix}0.0133\\ 0.0001\end{bmatrix}\end{aligned}\right\} \quad (8)$$

Table 1: Design parameters of POSLL Converter

Variable	Parameters	Values of POSLL Converter
L	Magnetizing inductance (µH)	100µH
C_1 & C_2	Capacitors (µF)	30µF
V_S	dc Input voltage source (V)	12V
P_o	Output power (W)	25.92W
f_s	Switching frequency (kHz)	100KHZ
R_o	Load resistance(Ω)	40-120Ω

IV. DISCRETE CONTROLLER DESIGN AND ANALYSIS

The design procedure follows three basic steps.

a) Design of a state feedback matrix to obtain stability by placing the closed loop poles appropriately on the left hand side of the z-plane.
b) Design of a suitable Load estimator in order to ensure the robustness.
c) Design of dynamic compensator using separation principle.

a. DESIGN OF DIGITAL STATE FEEDBACK MATRIX

The foremost idea is to design the digital state feedback gain matrix based on control law given by $u = -mx(k)$ for the POSLL converter. Step response is obtained to ensure the stability of the designed parameters. Initially root locus of POSLL converter is drawn and the desired closed loop poles are placed appropriately to obtain the digital state feedback matrix. The essential and satisfactory condition for the subjective pole placement of the system is that the system should be entirely controllable and it will be very much simpler to find the state feedback gain matrix when the state equations are in the controllable canonical form.

Here the closed loop poles are arbitrarily placed in z-plane for POSLL converter in such a way that the output, y (k) tracks any of the references r (k), which is considered as a unit step function in this case.

The simpler configuration for the design using state feedback method is illustrated in fig.3. In this method the state vector 'x' is measured rather than the output 'y'. The state vector thus measured is weighted by a constant feedback gain matrix, 'm' and the result is subtracted from the reference signal 'r'. The closed loop equations for a continuous time system are as follows:

$$\dot{x}(t+1) = Gx(t+1) + H(r - mx) = (G - Hm)x(t+1) + Br(t+1) \quad (9)$$

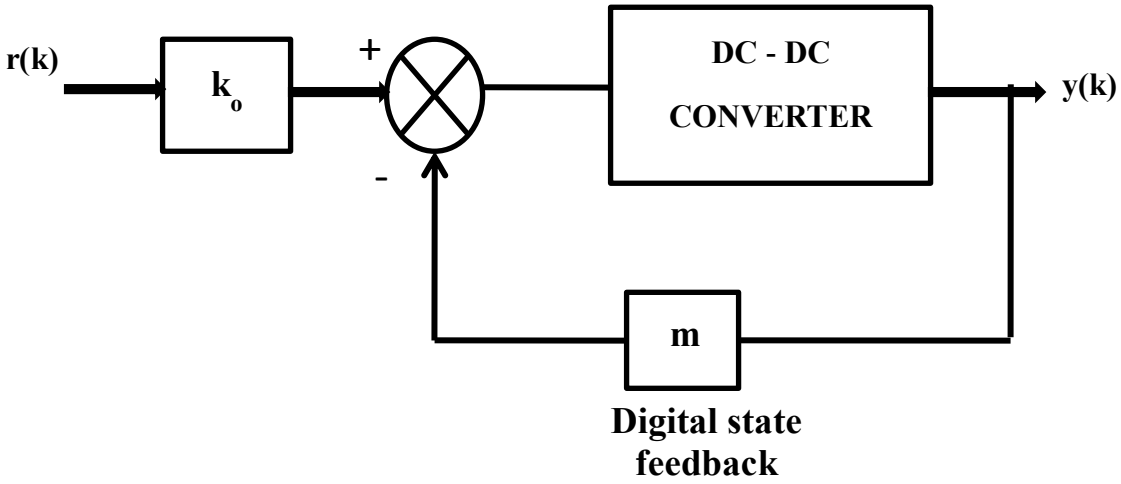

Fig.3 Control scheme for discrete time system

Here k_o represents the adjustable gain. Since we have considered a discrete time system, *t* is being replaced by *(t+1)* and let *t+1* be *k*. Thus equation (9) can be rewritten as,

$$\dot{x}(k) = (G - Hm)x(k) + Br(k) \qquad (10)$$

The output equation is given as follows,

$$y(k) = (C_d - D_d m)x(k) + C_d r(k) \qquad (11)$$

With the indispensable and adequate condition that the system should be completely state controllable, all the Eigen values of *(G-Hm)* are placed in the left half of z plane for the discrete time system. In controllable canonical form (G, H) pair is equivalent to $(\check{G}, \check{H})$ and it is given by,

$$\left.\begin{aligned} \check{G} &= \begin{bmatrix} 0 & 1 & 0 & \dots & 0 \\ 0 & 0 & 1 & \dots & 0 \\ \vdots & \vdots & \vdots & \vdots & \dots \\ -a_0 & -a_1 & -a_2 & \dots & -a_{n-1} \end{bmatrix} \\ \check{H} &= \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 1 \end{bmatrix} \end{aligned}\right\} \qquad (12)$$

It is essential to convert the system into reachable canonical form and the transformation matrix T_r which converts the POSLL converter system in to canonical form is given by the following equation,

$$T_r = [H \vdots GH \vdots \cdots \vdots G^{n-1}H] \begin{bmatrix} d_1 & d_2 & \dots & d_{n-1} & 1 \\ d_2 & d_3 & \dots & 1 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ d_{n-1} & 1 & 0 & \dots & 0 \\ 1 & 0 & 0 & \dots & 0 \end{bmatrix} \qquad (13)$$

Where $d_1, d_2 \dots d_n$ are the coefficients of the characteristic equation of the system given by,

$$z^n + d_1 z^{n-1} + \cdots + d_{n-1} z + d_n = 0 \qquad (14)$$

The closed loop system is formed by feeding back each state variable to u, forming,

$$u = -mx \qquad (15)$$

Where $m = [m_1 \quad m_2 \quad \dots \quad m_n]$ (16)

By using equation (10) with equations (12) and (16), the system matrix (G-Hm), for closed loop system is,

$$G - Hm = \begin{bmatrix} 0 & 1 & 0 & \dots & 0 \\ 0 & 0 & 1 & \dots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ -(d_0 + m_1) & -(d_1 + m_1) & -(d_2 + m_3) & \dots & -(d_{n-1} + m_n) \end{bmatrix} \quad (17)$$

Now the system equation is in controllable canonical form and hence by inspection the characteristic equation of the closed loop system is written as,

$$|zI - (G - Hm)| = z^n + (d_{n-1} + m_n)z^{n-1} + (d_{n-2} + m_{n-1})z^{n-2} + \cdots + (d_n + m_2)z + (d_0 + m_1) = 0 \quad (18)$$

By examining equations (14) and (18), it splendidly implicits that the closed loop characteristic equation of the system under controllable canonical form can be written by inspection from the open loop characteristic equation by adding the appropriate m_i to each coefficient. The desired characteristic equation of the system for suitable pole placement is assumed as,

$$z^n + \omega_{n-1}z^{n-1} + \omega_{n-1}z^{n-1} + \cdots + \omega_2 z^2 + \omega_1 z + \omega_0 = 0 \quad (19)$$

Where $\omega_i's$ are the desired coefficients. By comparing equations (18) and (19) it can be obtained as

$$\omega_i = d_i + m_{i+1}, i = 0,1,2, \dots n-1 \quad (20)$$

From which, $m_{i+1} = \omega_i - d_i$ (21)

Using the above steps the values for the state feedback matrices obtained for Positive Output super lift Luo converters are, $m = [99.4 \quad 6763.1]$. In order to ensure the robustness of the control law the unit step input is given to the system and the response is obtained as shown in the fig.4.

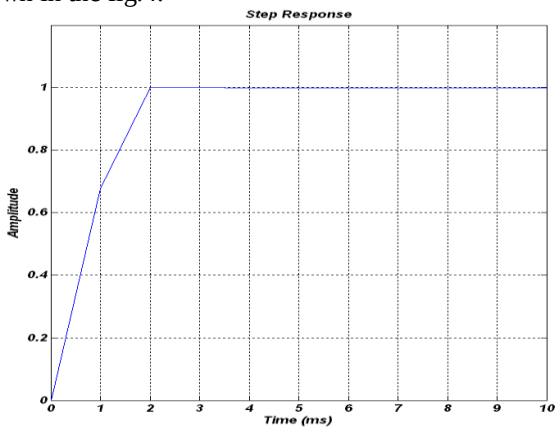

Fig.4 Response of the POSLL converter to the step input

The step response obtained for the POSLL converter guarantees that the digital state feedback gain matrix thus obtained makes the system more stable.

b. DESIGN OF THE LOAD ESTIMATOR

The load estimation is made by deriving the full order observer gain matrix. It is derived using the similar pole assignment procedure with the eventual objective of estimating the unmeasurable state parameters. The observer always aims to act upon the error resulting in faster response of the converter. The essential condition for the observer gain matrix design is that the dc-dc converter considered for the analysis should be completely state-observable. Hence for the appropriate location of the observer poles the following assumptions are made as defined by the thumb rule.

The natural frequency of oscillation (observer controller) is approximately equal to 2 to 5 times that of the natural frequency of oscillation of the system. Now, the active system equation along with a full-order state observer is described as follows:

$$\dot{x}(k+1) = (G - Hm)x(k) + Hm_1 r(k) \quad (22)$$

Here m_1 represents the coefficient of the state feedback matrix and r represents the step function.

The system equation along with the full order observer can be described by the following,

$$\tilde{x}(k+1) = G\tilde{x}(k) + Hu(k) + g\big(y(k) - C\tilde{x}(k)\big) \quad (23)$$

Here g represents the full order observer gain matrix.
Now the transfer function of the prediction observer controller, which is a combination of state feedback matrix and full order observer, is obtained using separation principle. It is given by,

$$\frac{U(s)}{-Y(s)} = \frac{795.4\,z - 721.5}{z^2 + 0.1027z + 0.03477} \quad (24)$$

Thus by separation principle the digital control law and the discrete state Observer can be designed separately and yet used together to provide a robust dynamic compensation for the second order system under consideration.

Table 2. Performance Evaluation of POSLL Converter with prediction Observer controller and **Output Response for Load Variations**

Sl.No.	Load Parameters			Reference Voltage (V)	Voltage across the load(V)
	R(Ω)	L(H)	E(V)		
1	100	--	--	36	36.00
2	110	--	--	36	35.97
3	110	100e-3	--	36	36.01
4	90	50e-3	--	36	35.98
5	105	50e-3	--	36	35.96
6	100	100e-3	--	36	36.00
7	100	100e-3	2	36	36.00

Sl. No	Performance Specifications	Discrete Controller	Analog Controller
1	Settling time (s)	0.005	0.5
2	Peak Overshoot (%)	0	0
3	Steady state error (V)	0	0.2
4	Rise time (s)	0.0025	0.1
5	Output Ripple Voltage	0	0

V. SIMULATION RESULTS

An appealing imminent into the dynamic performance of the POSLL converter along with discrete observer controller is obtained by carrying out an extensive simulation using MATLAB/Simulink. The results thus obtained are illustrated in Table 2. It is observed that the closed
loop system exhibits an improved dynamic response with a settling time of the order of just 0.005s.There
are no overshoots and undershoots. The system also executes splendidly with zero steady state error and output ripple voltage. Table 2 also exemplies the parameters in comparison with its analog counterpart. It is evident that the POSLL converter with prediction observer shows better results. Again the input voltage and load resistance are varied over a range of 10% to 20% and the results thus obtained are illustrated in fig.5.

It is found that the output response shows good dynamic performance irrespective of the line and load disturbances. The system settles faster and the simulation results very well match with the mathematical computations and thus a stiff output regulation is obtained. The converter along with the controller is capable of tracking the output voltage of 36V, inspite its line and load disturbances. The output response of the converter with load variations is illustrated in table 2. The results show that the system is dynamic and robust. By analyzing the performance it is understood that the POSLL converter with discrete controller demonstrates enhanced performance than its analog counterpart.

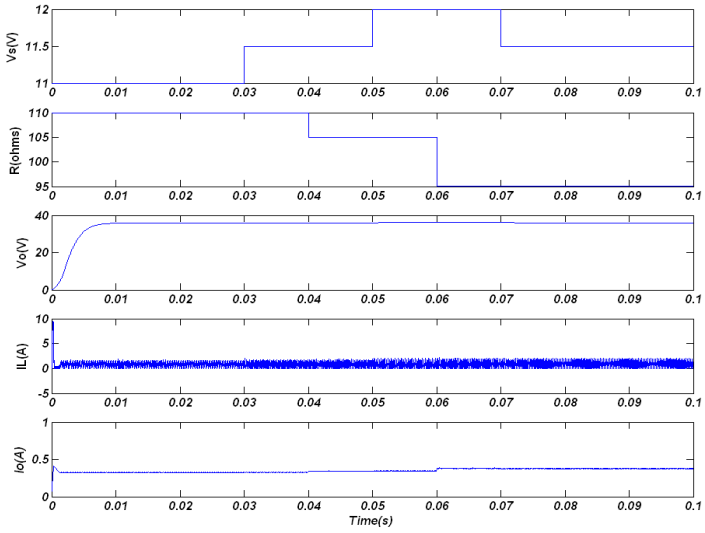

Fig.5 Output Response of POSLL converter (Vs – input voltage, R – Load Resistance, V_O – Output Voltage, I_L –current through the inductance, I_O – Load current)

Since the Observer is mainly proposed to verify the robustness of the control law, it is necessary that the estimated error variables should converge at zero from any non zero initial value. This ensures the asymptotic stability of the system under consideration with the desired pole locations. It is expressed in the Figs.6 (a) and 6(b). The error variables for the designed system thus converge at zero thereby ensuring the stability of the system.

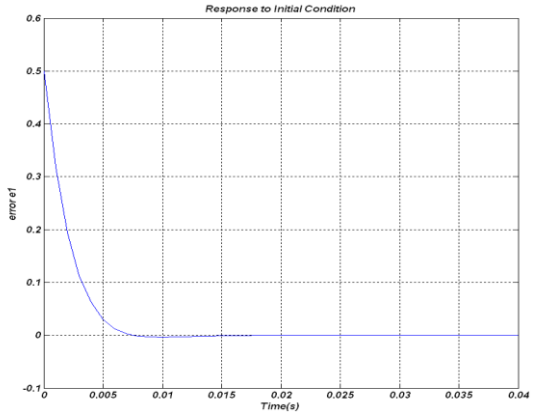

Fig. 6(a) Estimation of error 1

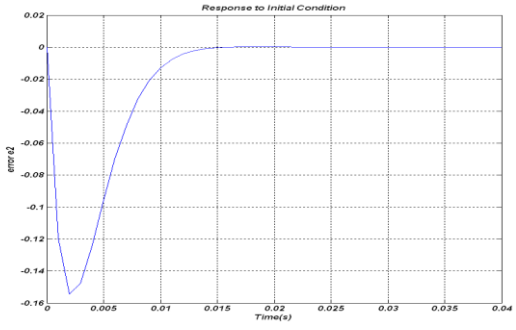

Fig. 6(b) Estimation of error 2

VI. Hardware Results

The controller platform is evaluated using dsPIC30F4011. The prototype is developed using the same values shown in table 1 and it is shown in fig.7.dsPIC30F4011 is a single chip ingrained controller which amalgamates the control characteristics of Microcontroller with the calculation and credentials of a Digital Signal Processor in a solitary core. It is a very powerful Microcontroller unit which executes all the instructions in a minimum time of about 33ns.It is a high performance controller which has CPU with several advanced features like, instruction sets optimized by the C compiler, most broad data path of about 16 bit, extensive instruction path of 24 bit and 84 base instructions. It comprises of 40 programmable digital I/O pins. It consists of an Enhanced Flash program memory of about 10,000 erase/write cycle for industrial temperature range of 100K and a Data EPROM memory of 100,000 erase/write cycle for industrial temperature range of 1M. The A/D converter is 10-bit with 4 S/H inputs, with 500Ksps conversion rate, 9 input channels. The A/D conversion is available during sleep mode as well as the idle mode. The experimental set up is shown in the fig.7.The corresponding outputs obtained are shown in the fig.8 and fig.9 respectively. Fig.8 shows the output corresponding to the line variation and it proves that the POSLL converter along with observer controller powerfully tracks the reference voltage of about 36V. Overshoots are evident which is very minimum and of appreciable order. Fig.9 illustrates the output corresponding to load variation.

Fig.7 Prototype model of the POSLL

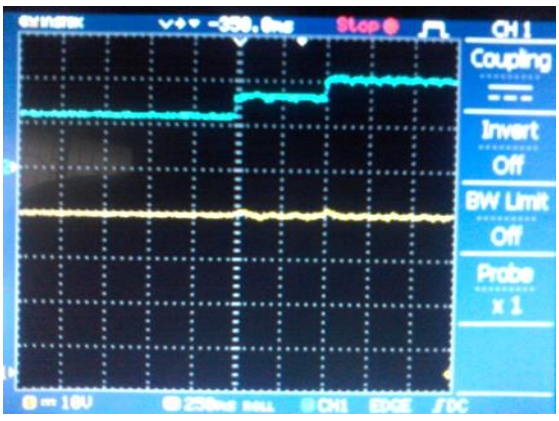

Fig.8 Output response for converter with Prediction Observer controller step change in input voltage of 10V, 12V, 14V

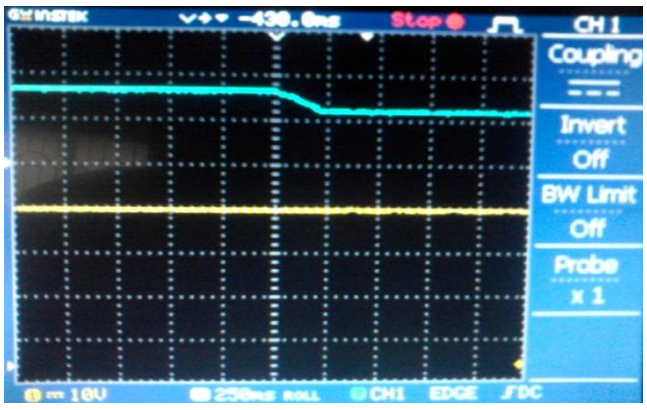

Fig.9 Output response for load change from 120Ω to 110

VII. CONCLUSION

Prediction Observer controller is designed and analysed for the Positive Output Super Lift Luo converter in Continuous time domain by means of pole assignment method and separation principle. In order to ensure the robustness of the Controller load estimator is derived using full order state Observer. The investigation and analysis are carried out using root locus method which endows with a competent and effectual compensation for the dc-dc converter. The prediction observer controller thus designed for the POSLL converter is realized using dsPIC30F4011 as a control platform and the outcomes are demonstrated. The numerical examination, simulation and experimental study show that the Prediction Observer controller designed for POSLL converter accomplishes rigid output voltage regulation, excellent dynamic characteristics and better efficiency. The POSLL converter with prediction observer controller can be used for any of the applications like modern portable electronic devices, computer peripherals, medical equipments, power factor correction or fuel cell applications

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