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Implementation Of 32-Bit Kogge-Stone Adder Using FPGA Technology

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***Abstract**-- The binary adder is the basic component in most computerized circuit outlines including advanced sign processors(DSP) and in data paths of microprocessor units. The extensive research continues to be focused on improving the power delay performance of the adder. In VLSI usage, Parallel prefix adders are known to have the best performance. Among the parallel prefix adders Kogge-Stone adder (KSA) has reduced power consumption and high speed. This paper explores the 32-bit KSA with modification in its architecture. The analysis of original KSA architecture and the modified KSA is compared and results are calculated. This project is carried out using the SPARTAN-3 and the software tool XILINX version 14.5. Simulation is carried out using ISIM.*

***Keywords-** Kogge-Stone adder, FPGA, Power, Verilog, Xilinx 14.5*

I.INTRODUCTION

The binary addition is that the fundamental math operation in the advanced circuits and it got to be key in the vast majority of the digital systems together with the ALU units, microprocessors and digital signal processing modules[3]. In the several applications like the in the mobile and telecommunication, the power and the speed is the major concern. All the user tend to opt those mobiles which have faster processor in it, such that the usage of these mobiles will be convenient for the users. So this can be achieved only by using faster processors that implies the faster ALU units which has the faster operation of the adder. As adder being the basic building blocks of any of the system. It's the duty of the designer to make sure that the adder which he has designed has got the reduced power consumption, less delay and less area. As there will be tradeoff between area, power and delay. We cannot reduce all 3factors at a time so designer can concentrate on oany of the one factor. The proposed project aims at the reduction of the power.

II.BASICS OF ADDER

The design of adders basically started from the half adder. With two inputs as A and B and the output as the Sum and carry. This was the basic adder which ever designer used in to add the numbers. The equations of the sum and carry is,

Sum S= A xor B (1)

Carry C= A and B (2)

The block diagram of the half adder (HA) is as shown in fig 1.

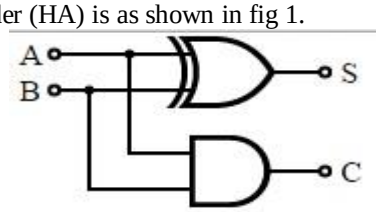

Fig 1. Basic block diagram of Half Adder.

After half adder , the full adder came in to existence. The full adder(FA) adds up three binary numbers as A,B and Cin ,and Sum Carry as the output to the adder. The equations of the FA is as follows,

Sum= A xor B xor Cin (3)

Carry= (A and B)+(B and Cin)+(A and Cin) (4)

The block diagram is as shown in fig 2.

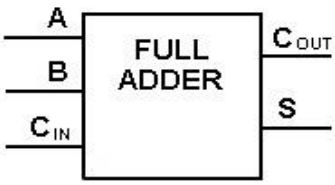

Fig 2. 1Bit Full Adder

Cascading of full adders lead to the ripple carry adder. The ripple carry adder is adopted from the full adder only. This was invented to carry out the addition operation for more numbers of bits. The major disadvantage of ripple carry adder is the carry bits are ripple thus the propagation of the carry signals lead to more delay. Because of the propagation delay ripple carry adder found to slow down in its operation. The block diagram of the ripple carry adder is as shown in the following fig 3.

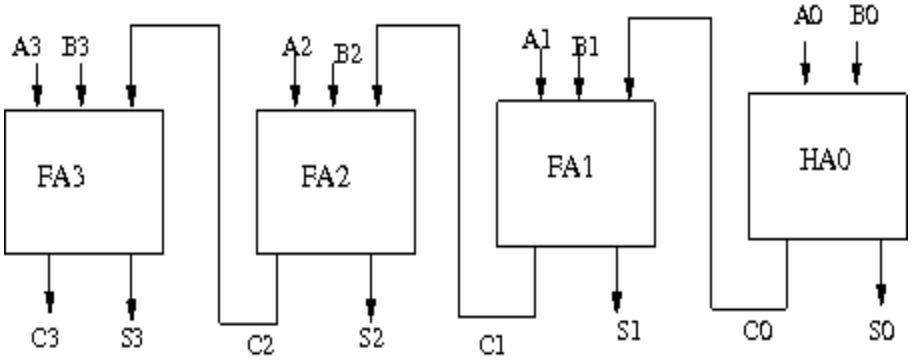

Fig 3. 4-bit ripple Carry Adder.

To overcome the disadvantages of the ripple carry adder the Carry look ahead(CLA) adder came into existence. The main flaw of the ripple carry adder was the propagation delay, this CLA washed away the flaws of ripple carry adder. To reduce the computation time, they designed CLA. It works by creating the two signals (P and G) for each bit position . Thus the speed of the CLA is more than the ripple carry adder. But the disadvantages of CLA is it consumes more area.

To overcome the drawback of these conventional adders. The parallel prefix adder came in to existence.

III . PARALLEL PREFIX ADDER

The PPA is like a Carry Look Ahead Adder. The production of the carriers the prefix adders can be designed in many different ways based on the different requirements. We use tree structure form to increase the speed of arithmetic operation. Parallel prefix adders are faster adders and these are faster adders and used for high performance arithmetic structures in industries. The parallel prefix addition is done in 3 steps.[2]

1. Pre-processing stage
2. Carry generation network
3. Post processing stage

a. Pre-processing stage

In this stage we compute, the generate and propagate signals are used to generate carry input of each adder. A and B are inputs. These signals are given by the equation 5&6.

Pi=Ai xor Bi. (5)

GI=Ai and Bi (6)

b. Carry generation network

In this stage we compute carries corresponding to each bit. Execution is done in parallel form [4].After the computation of carries in parallel they are divided into smaller pieces. carry operator contain two AND gates , one OR gate. It uses propagate and generate as intermediate signals which are given by the equations 7&8.

$P(i:k) = P(i:j) \cdot P(j-1:k)$. (7)

$G(i:k) = G(i:j) + (G(j-1:k) \cdot P(i:j))$. (8)

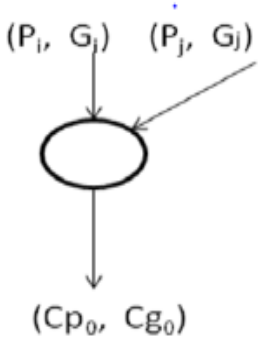

Fig 5. Shows the carry operator

c. Post processing stage

This is the final stage to compute the summation of input bits. it is same for all adders and sum bit equation given

Si= Pi xor Ci (9)

Ci+1=(Pi .C0) + Gi (10)

The discussed stages in this section is represented in a block diagram.

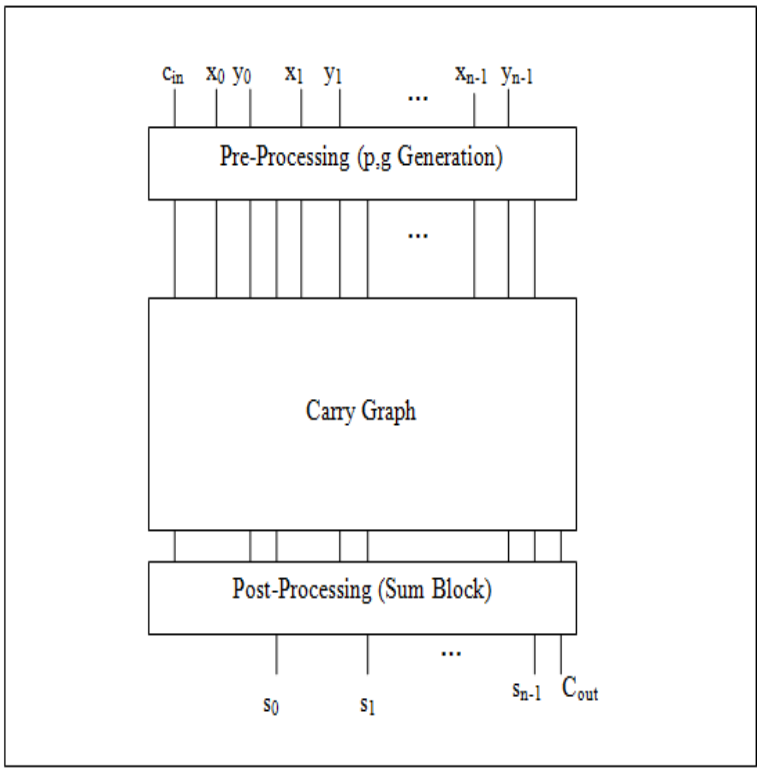

Fig 4. Parallel prefix adder stages

Parallel Prefix Adders are classified into many types among those,

1. Kogge- Stone Adder
2. Brent-Kung Adder
3. Ladner-Fischer Adder.

1.Kogge Stone Adder

The Kogge Stone Adder (KSA) has regular layout which makes them favored adder in the electronic technology. Another reason the KSA is the favored adder is because of its minimum fan-out or minimum logic depth. As a result of that, the KSA becomes a fast adder but has a large area . The delay of KSA is equal to *log2n* which is the number of stages for the "*o*" operator. The KSA has the area (number of "*o*" operators) of *(n*log2n)-n+1* where *n* is the number of input bits.[1]

2. Brent Kung Adder

The large number of levels in Brent Kung Adder (BKA) however reduces its operational speed. BKA is also power efficient because of its lowest area delay with large number of input bits. The delay of BKA is equal to *(2*log2n)-2* which is also the number of stages for the *"o"* operator. The BKA has the area (number of *"o"* operators) of *(2*n)-2-log2n* where *n* is the number of input bits. The BKA is known for its high logic depth with minimum area characteristics. High logic depth here means high fan-out characteristics[1]

3.Ladner-Fischer Adder

Ladner- Fischer adder is a parallel prefix adder. This was developed by R. Ladner and M. Fischer in 1980.Ladner- Fischer adder[6] has minimum logic depth but it has large fan-out . Ladner- Fischer adder has carry operator nodes.

In terms of area or cost between the two PPAs, the BKA proves to be a better choice. Even though the BKA's area rises as the bit size increase, it does not rise as drastically as KSA. The higher the number of bits supported by the PPAs, the bigger is the adder in terms of area. In terms of computational delay or time propagation delay (*tpd*), KSA is a better choice. Although BKA has lower *tpd* for bit size of 8 bits, the KSA has very low *tpd* compared to BKA when the bit size is more than 16 bits. Therefore, only at bit size less than 16 bits the KSA has longer *tpd*. The KSA is widely-known as a PPA that performs fast logical addition.

Let's get to the implementation of Kogge stone adder .Below shows the 32-bit KSA

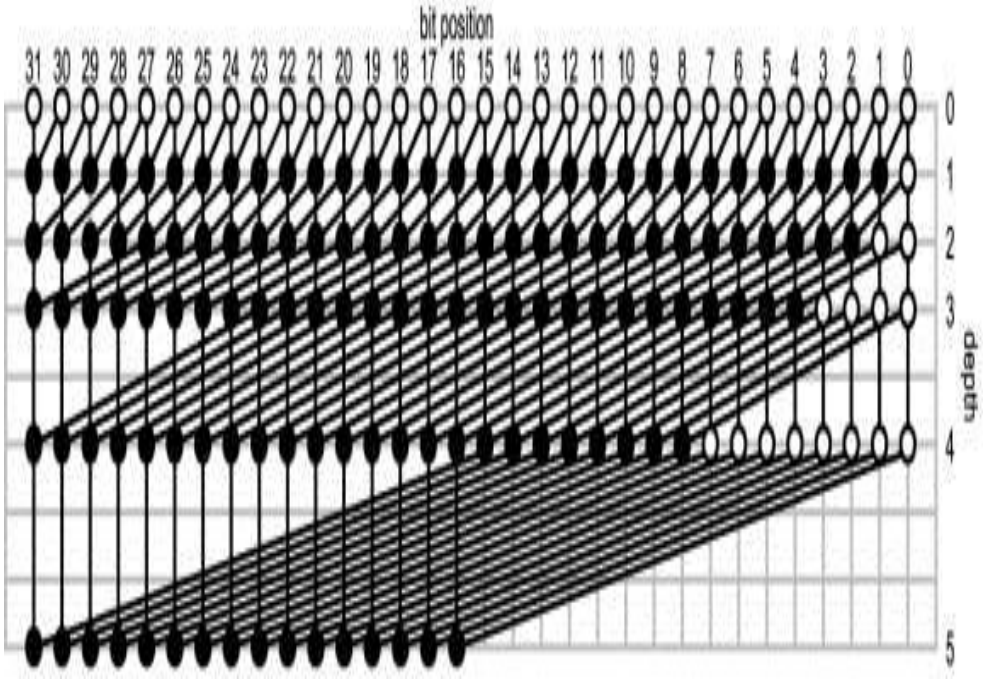

Fig 5. 32-bit Kogge-Stone adder

IV.Modified 32BIT- Kogge-Stone Adder

The main motto of the proposed project is to reduce the power consumption of existing Kogge-stone adder. A novel work has been done to reduce the power by changing the architecture of the Kogge-stone adder. This modification is with respect to the architectural level of original KSA. In the original KSA the designer had used the XOR gate for the calculation of propagation (P) signal and the sum(S). But if we replace this XOR gate with the 2:1MUX the operation of the adder remains same but the power consumed by the KSA is reduced.

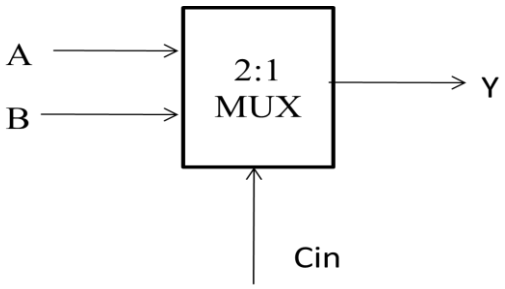

Fig 6. 2:1MUX

The formulas and the stages of the KSA remains same as that of Original KSA. For the

a. Pre-processing stage
   Pi=Ai xor Bi.
   GI=Ai and Bi.
   But the XOR gate is replaced by the MUX
b. Carry generation stage
   P(i:k) =P(i:j) **.** P(j-1:k).
   G(i:k) =G(i:j) +(G(j-1:k) **.** P(i:j)).
   For the calculation of the intermediate signals P and G.
c. Post-processing stage.
   Si= Pi xor Ci
   Ci+1=(Pi **.**C0) + Gi
   For the generation of sum and carry I,e the results.

By replacing the XOR gate with 2:1MUX, the power will be reduced. The modified architecture of KSA is shown in the fig 7.

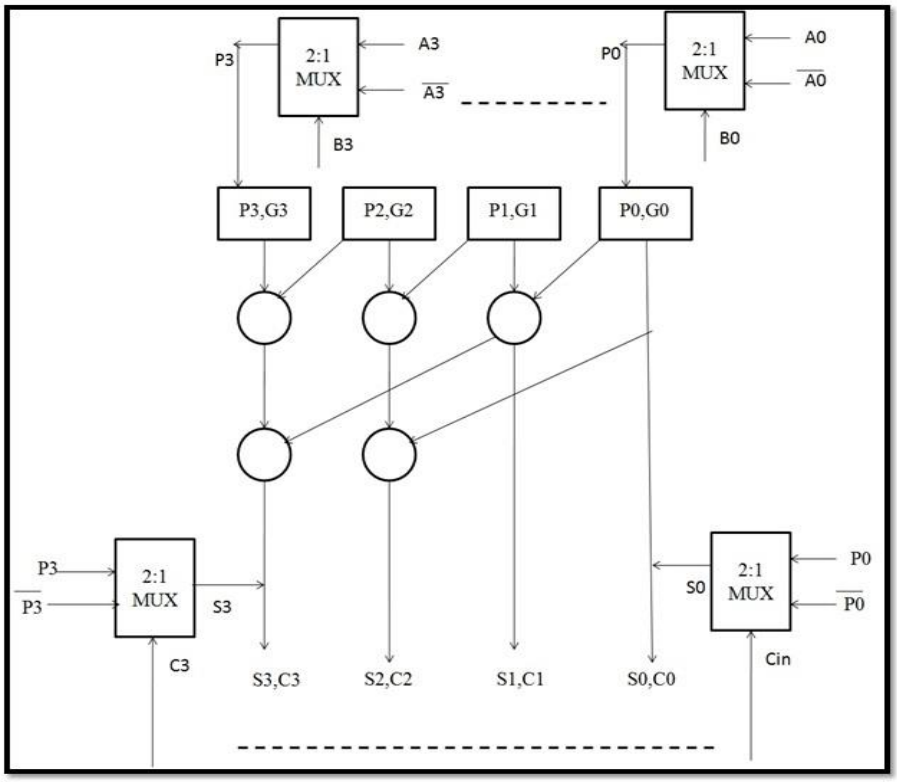

Fig 7. Modified architecture of 4-Bit KSA

This modified KSA block diagram can be extended to further higher bits i,e 8,16 and 32bits. The proposed modified architecture is implemented to 32-bits on the Xilinx tool in this project .

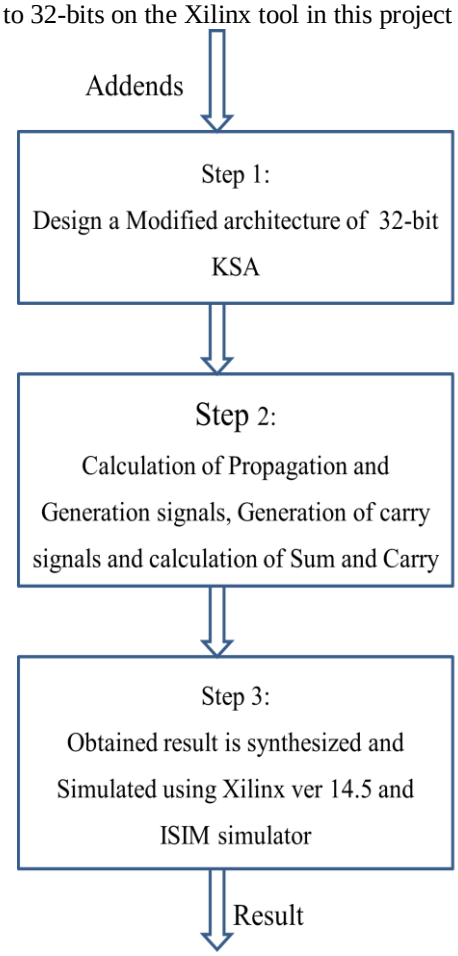

Fig 8. Flow diagram of Modified 32-BIT Kogge-Stone adder.

The above flow diagram fig 8.shows the methodology for the proposed 32-bit KSA. The designed program as well as the calculation of the result is verified with respect to the tool Xilinx

V.RESULTS AND ANALYSIS

A. Simulation Results

The RTL schematics of 32-Bit KSA is as shown below in the fig.10. the proposed KSA architecture has 3stages as discussed in the above section. With respect to the KSA modified architecture the program has veen designed and the RTL is generated.

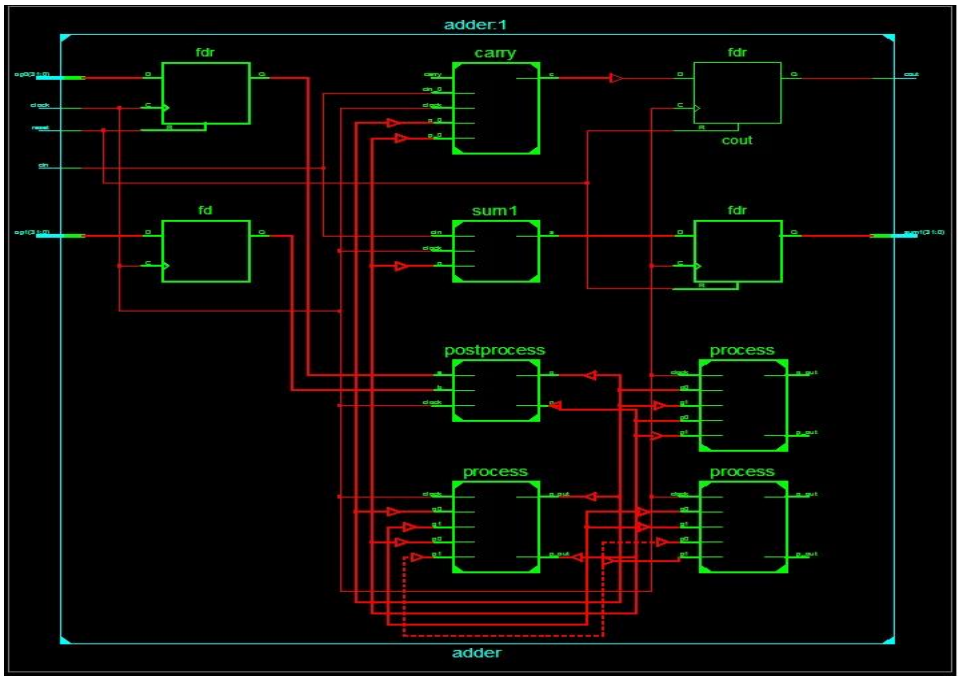

Fig 10. RTL schematic of 32-Bit Kogge-Stone adder.

The simulated result of 32-Bit KSA adder as shown in the fig 11. The computation of KSA is done using the tool ISIM(simulator)

Fig 9. Shows the simulated result of the 32-Bit Kogge-Stone adder.

Where op0= 12345678
op1= +87654321

Sum1= 99999999
Cout=0

In the fig 9. The representation of the number is done in the binary. This binary is explained in the decimal numbers.

B. Power Analysis

ADDER	Power(mW)
Kogge-Stone adder with Xor	42.01
Kogge-Stone adder with Mux	41.42

Table 1. Power analysis of KSA with Xor and Mux

This reduction of the power is because of using the xor gate in the architecture of the original KSA. Thus leading to the power reduction.

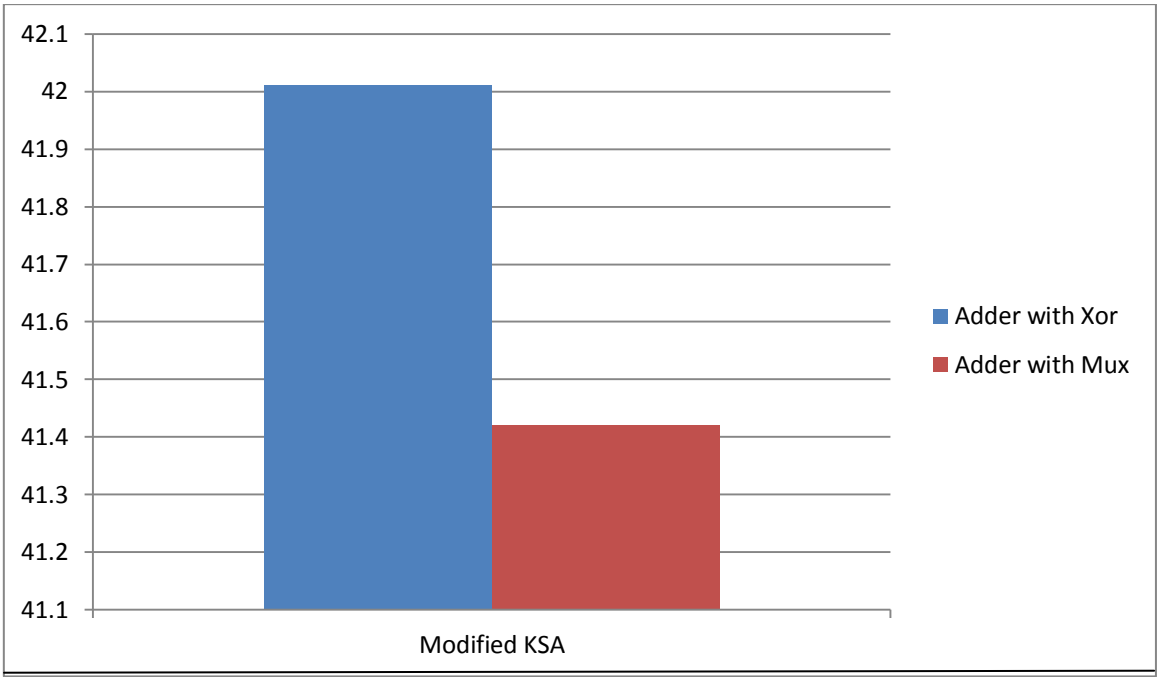

Fig 10. Shows the Bar-graph of Modified KSA power analysis.

VI.CONCULSION

This paper presents a novel work on the KSA. An attempt has been made to reduce the power of KSA by changing the architecture of the original KSA. The proposed architecture proves that using the mux in the KSA instead of xor will reduce the power consumption of the adder. This proposed architecture can not only be implemented on the tool, this can be implemented on the silicon. Thus the Kogge-stone adder has reduced power than any other parallel prefix adders.

FUTURE SCOPE

The proposed 32-bit Kogge-Stone adder can be extended to further higher bits. So that this KSA can be made use for the higher order bits depending n the application of the user.

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