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# Design And Performance Analysis Of 8x8 Vedic Multiplier Using Submicron Technology

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***Abstract* --** Multiplication is one of the basic operations for any high speed digital logic system design, digital signal processors or communication system. Primary issues in design of multiplier are area, delay, and power dissipation. There are many algorithms like booth multiplier, array multiplier, vedic multiplier, compressor based vedic multiplier for overcoming this problems. This paper mainly presents VEDIC multiplier using Urdhva Tiryagbhyam Sutra and it uses Full Adder, Ripple Carry Adder, and basic gates. The design has been implemented using 45nm CMOS and GDI technology at 1.0v supply voltage in LTSpice IV tool.

***Index Terms*** — Vedic Multiplier, Urdhva Tiryagbhyam Sutra, CMOS 45nm Technology, Gate Diffusion Input, GDI 45nm Technology, Ripple Carry Adder, Simulation Results, Comparison.

## I. INTRODUCTION

Multiplier is one of the common operations that are widely used in many digital signal processors, communication systems, encryption and decryption algorithms. A general multiplier block consists of AND gates to generate the partial products and ADDERS to add these partial products. But as the number of bits that are to be multiplied increases, the need for ADDER blocks increase. This would in turn result in a delay due to long ADDER tree structure. Besides this power consumption by the typical multiplier is also the major issue that needs to be concerned. Thus, to eliminate these problems the nonconventional ancient method of Vedic mathematics has been adopted in this paper.

The Vedic mathematics comprises of 16 different Vedic sutras called Vedic formulae, which are used to solve a wide range of mathematical problems. These sutras save a lot of time as compared to conventional computations.

This paper proposes 8x8 Vedic multiplier using Urdhva Tiryagbhyam sutra of Vedic mathematics and uses CMOS 45NM and Gate Diffusion Input (GDI) 45NM technology which is implemented in LTSpice IV tool. The rest of paper is organized as follows. Section II gives the methodology of Vedic multiplication technique. Section III gives the proposed multiplier architecture. Section IV gives future work and conclusion.

## II. VEDIC MULTIPLICATION METHOD

The use of Vedic mathematics provides reduced calculations and reduced delay in conventional mathematic problems. This is because the Vedic mathematics is based on the principles on which algorithms are implemented as human minds interpret.

Out of 16 Vedic sutras given by ancient mathematics, the formulae which are being used for the purpose of multiplication are 1) Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10 and 2) Urdhva-tiryagbyham – Vertically and crosswise.

### A. Urdhva Tiryagbhyam Sutra

As the multiplication operation in UT sutra is computed parallel the delay in output is significantly reduced. The sutra is also known as 'vertically and crosswise'. Initially the UT sutra was used for decimal numbers only. However it can also be used for binary numbers. The method how binary multiplication is done using UT method for 2-bit, 3-bit and 4-bit numbers is shown in Fig. 1.

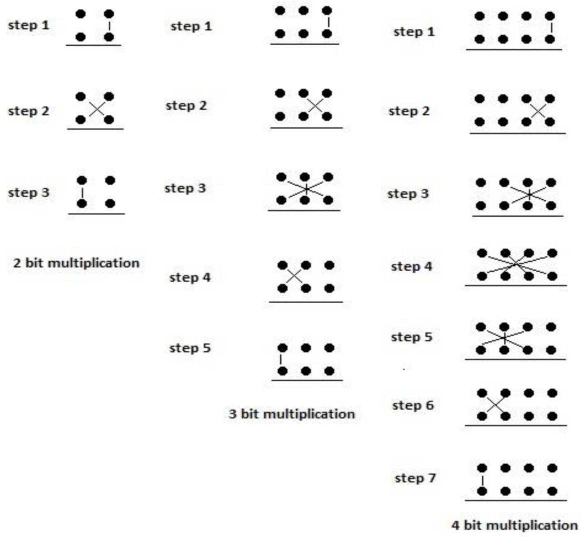


*Fig.1. UT Method for 2,3,4 bit numbers*

Since the partial products and their sums are calculated independently, the multiplier is independent of the clock of the processor. The delay is generated only due to the occurrence of carry from the partial products which is needed to be added in each next step's partial product.

## III. PROPOSED MULTIPLIER ARCHITECTURE

The proposed architecture for 2X2, 4x4 and 8x8 bit Vedic multiplier are shown in the below sections. Here, "Urdhva-Tiryagbhyam" (Vertically and Crosswise) sutra is used to for the multiplication of two binary numbers. It utilizes only logical AND gate, XOR gate as basic function and some modification to create full adders and ripple carry adders from these gates for extending the multiplier bits from 2x2 to 4x4 and 8x8 bits multiplier.

### A. CMOS Logic

CMOS combines NMOS and PMOS transistors in a structure which consists of a Pull-Up Network (PUN) and a Pull-Down Network (PDN) to implement logic functions. PUN and PDN are duals of each other.
A current path (connection) from VDD to VF means VF is high (f is logic 1). A current path (connection) from VF to GND means VF is low (f is logic 0). "AND" corresponds to transistors in series. "OR" corresponds to transistors in parallel.

### B. Gate Diffusion Input Logic

Using GDI technique, implementation of a wide range of complex logic functions is possible using only two transistors. GDI technique is based on the use of a simple cell which looks like standard CMOS inverter as shown in fig. 3.

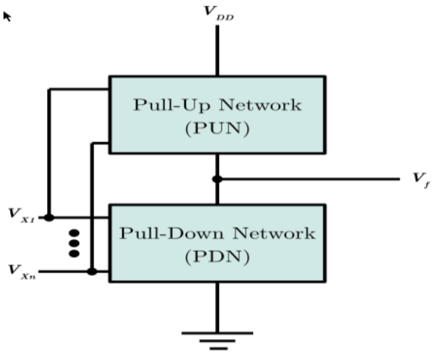


*Fig.2. CMOS Architecture*

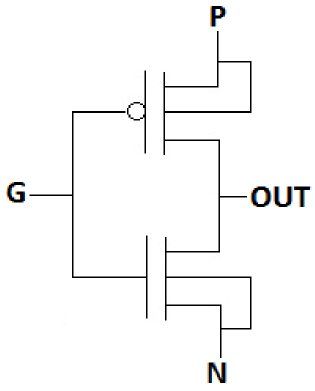


*Fig.3. GDI Basic Cell*

(1) GDI cell consists of 3 inputs. G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS) and N (input to the source/drain of nMOS).
(2) N or P (respectively) are connected to bulks of both nMOS and pMOS, so it's biasing can be done arbitrarily at contrast with CMOS inverter.

GDI technique is suitable for design of efficient low power circuits. It uses a reduced number of transistors as compared to CMOS. At the same time, it improves logic level swing and static power characteristics and allows simple top-down design by using small cell library. TABLE I shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions.

TABLE I
VARIOUS FUNCTIONS OF GDI CELL USING DIFFERENT CONFIGURATIONS

| N | P | G | D | FUNCTION |
|---|---|---|---|---|
| 0 | B | A | Ā | F1 |
| B | 1 | A | Ā+B | F2 |
| 1 | B | A | A+B | OR |
| B | 0 | A | AB | AND |
| C | B | A | ĀB+AC | MUX |
| 0 | 1 | A | Ā | NOT |

These functions are very complex when implemented in CMOS logic and require 6-12 transistors. But the same functions are very easy to implement using GDI method and require only two transistors per function.

### C. Implementation of AND gate Using CMOS and GDI

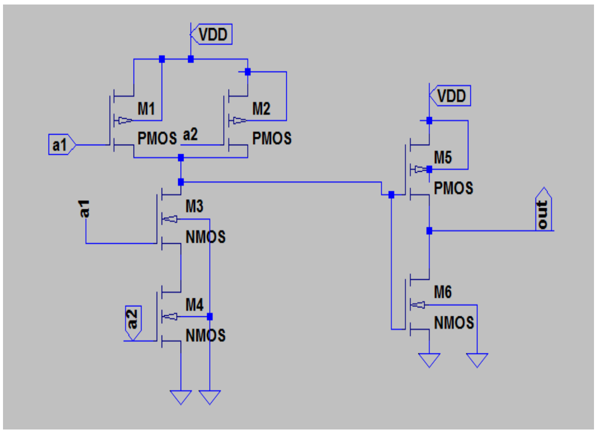


*Fig.4. AND gate using CMOS*

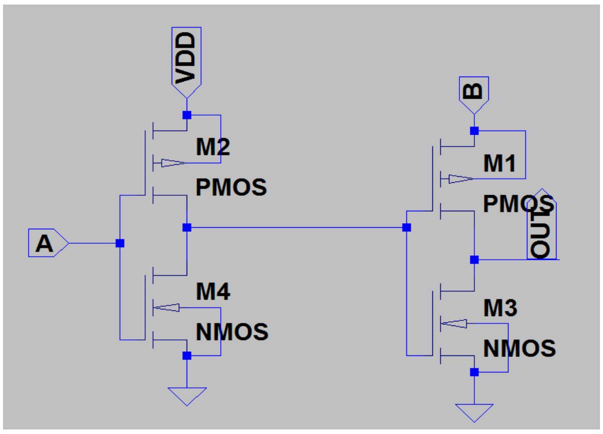


*Fig.5. Modified AND Gate with Inverter*

The AND gate implementation with CMOS logic is shown in the Fig.4.The AND gate implementation using GDI Logic normally is composed of two transistors Fig.5. However to increase the waveform shaping at output the modified design has been used for implementation. Thus it will improve the output results at a cost of increased transistors, power consumption and area occupied. The same procedure has been carried out for implementation of GDI XOR gate. In turn the full-adder and ripple carry adder blocks are made of AND gates and XOR gates, the overall power consumption and delay will be more than earlier GDI logic.

### D. OR Gate using CMOS and GDI Logic

The OR gate using CMOS is made up of four transistors plus inverter, while Normal Gate Diffusion Input logic consists of two transistors, which is not shown here. However the schematic has been modified with the use of inverter which is shown in fig. 7.

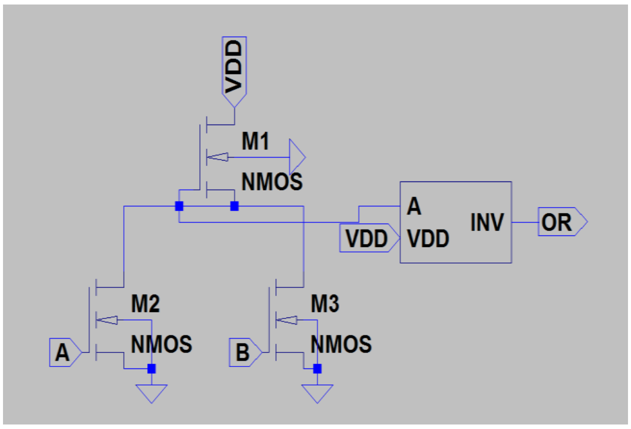


*Fig.6. OR gate using CMOS*

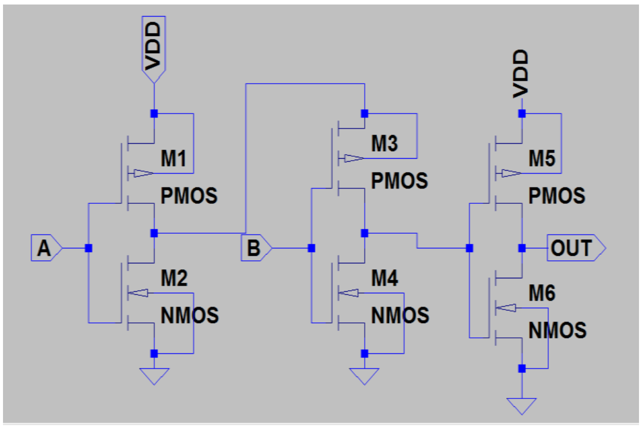
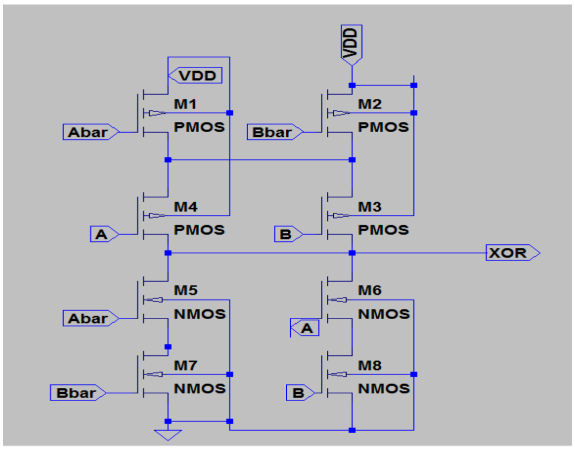


*Fig.7. Modified OR gate with Inverter*

### E. XOR Gate using CMOS and GDI



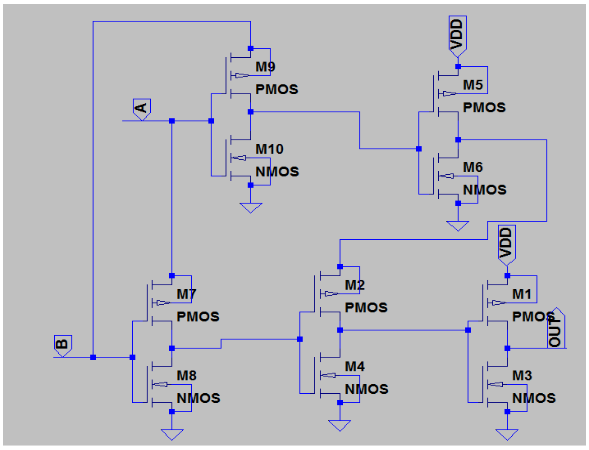


*Fig.8 XOR gate using CMOS* *Fig.9. Modified XOR Gate with Inverter*

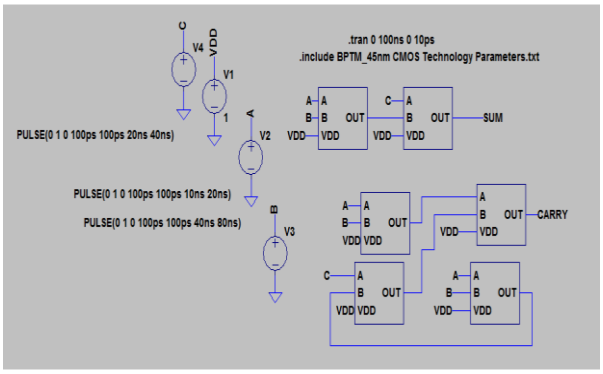
XOR gate CMOS implementation in general consists of 8 transistors and two inverters. The XOR gate using GDI with 10 transistors is shown in Fig. 9.

### F. Full Adder

The full adder schematic shown in above Fig.10 uses XOR gates, AND gates and OR gates which are already implemented and their symbols are used as their logical working. Both the CMOS and GDI logic's schematic will be the same as shown in figure.

### G. Ripple Carry Adder

The ripple carry adder uses the full adder as basic building block. The carry from the full adder block is transferred to the next adder block which is shown in the fig.11.


C
V4
VDD
V1
1
A
V2
B
V3
PULSE(0 1 0 100ps 100ps 20ns 40ns)
PULSE(0 1 0 100ps 100ps 10ns 20ns)
PULSE(0 1 0 100ps 100ps 40ns 80ns)
.tran 0 100ns 0 10ps
.include BPTM_45nm CMOS Technology Parameters.txt
A
B
OUT
VDD
C
SUM
CARRY

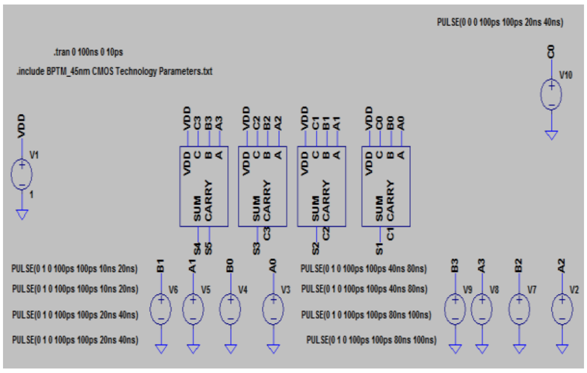

PULSE(0 0 0 100ps 100ps 20ns 40ns)
.tran 0 100ns 0 10ps
.include BPTM_45nm CMOS Technology Parameters.txt
C0
V10
VDD
V1
1
VDD C3 B3 A3
VDD C2 B2 A2
VDD C1 B1 A1
VDD C0 B0 A0
VDD C B A
SUM
CARRY
S4 S5
S3 C3
S2 C2
S1 C1
PULSE(0 1 0 100ps 100ps 10ns 20ns)
PULSE(0 1 0 100ps 100ps 10ns 20ns)
PULSE(0 1 0 100ps 100ps 20ns 40ns)
PULSE(0 1 0 100ps 100ps 20ns 40ns)
B1
V6
A1
V5
B0
V4
A0
V3
PULSE(0 1 0 100ps 100ps 40ns 80ns)
PULSE(0 1 0 100ps 100ps 40ns 80ns)
PULSE(0 1 0 100ps 100ps 80ns 100ns)
PULSE(0 1 0 100ps 100ps 80ns 100ns)
B3
V9
A3
V8
B2
V7
A2
V2

*Fig.10. Full Adder using Inverter* *Fig.11. 4bit Ripple Carry Adder*

### H. 2x2 bits Vedic Multiplier

Consider the following two, 2 bit numbers A and B where A = a1a0 and B = b1b0. Firstly, the least significant bits a0 and b0 are multiplied which gives the least significant bit s0 of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit s1 of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum s2 and carry c2. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

s0 = a0b0………………….. (1.1)
c1s1 = a1b0 + a0b1……….... (1.2)
c2s2 = c1 + a1b1………….... (1.3)

The final result will be c2s2s1s0. This multiplication method is applicable for all the cases. (1.1), (1.2) and (1.3) show that the 2X2 multiplier requires four AND gates & two half-adders which is displayed in its block diagram in Fig.12.

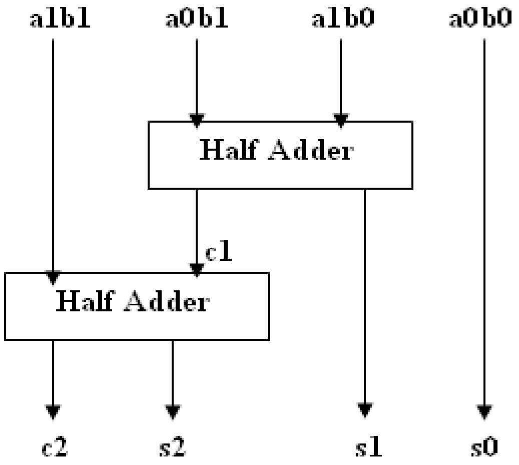
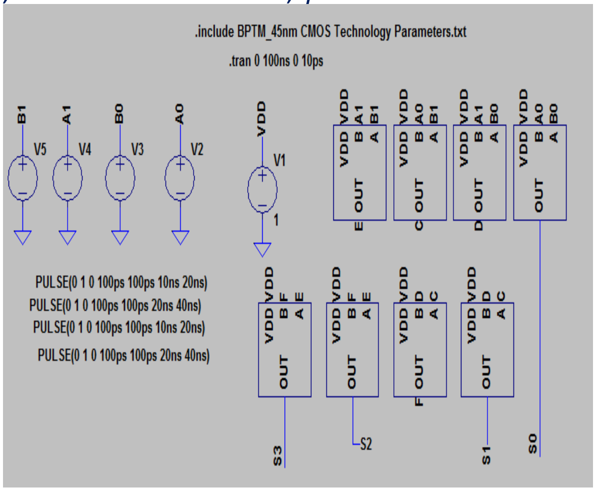


Fig.12. Block Diagram of 2x2 Multiplier



```
.include BPTM_45nm CMOS Technology Parameters.txt
.tran 0 100ns 0 10ps
```

```
PULSE(0 1 0 100ps 100ps 10ns 20ns)
PULSE(0 1 0 100ps 100ps 20ns 40ns)
PULSE(0 1 0 100ps 100ps 10ns 20ns)
PULSE(0 1 0 100ps 100ps 20ns 40ns)
```

Fig.13. Schematic of 2x2 multiplier

## I. Vedic Multiplier for 4x4 bit Module

The 4x4 bit Vedic multiplier is implemented using four 2x2 bit Vedic multiplier blocks as discussed in Fig.14. Let's assume the two 4 bit numbers, say A= A3 A2 A1 A0 and B= B3 B2 B1 B0. The output line for the multiplication result is – S7 S6 S5 S4 S3 S2 S1 S0. To get final result of multiplications (S7 - S0), four 2x2 bit Vedic multipliers and three 4-bit Ripple-Carry (RC) Adders are necessary. The RC Adders are made up of full adders, which help us to reduce delay. Similarly, 8x8 Vedic multiplier modules can be implemented easily by using four 4x4 multiplier blocks.

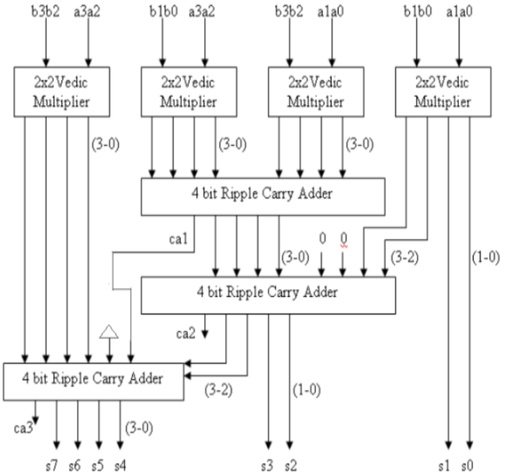


Fig.14. 4x4 Multiplier Architecture

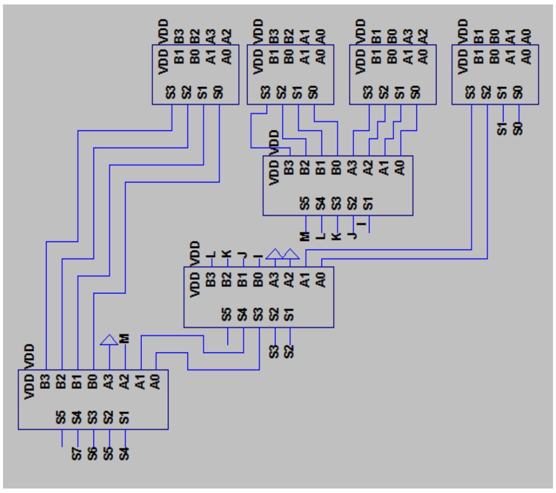


Fig.15. Schematic of 4x4 Multiplier

## J. Vedic Multiplier for 8x8 bit Module

The 8x8 bit Vedic multiplier can be easily implemented by using four 4x4 bit Vedic multiplier blocks as shown in the block diagram in Fig.16. In multiplication result the output bits will be of 16 bits as – S15 - S0. Here total three 8 bit Ripple-Carry Adders are required as shown in Fig.16.

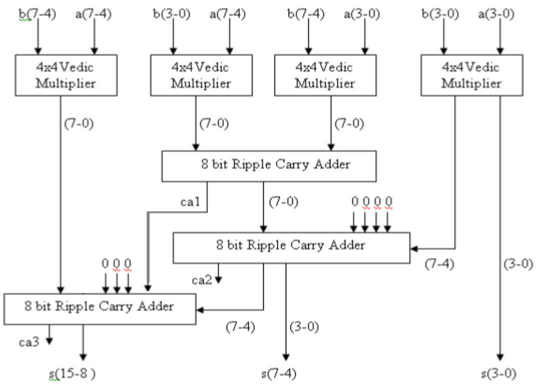


Fig.16. Architecture of 8x8 multiplier

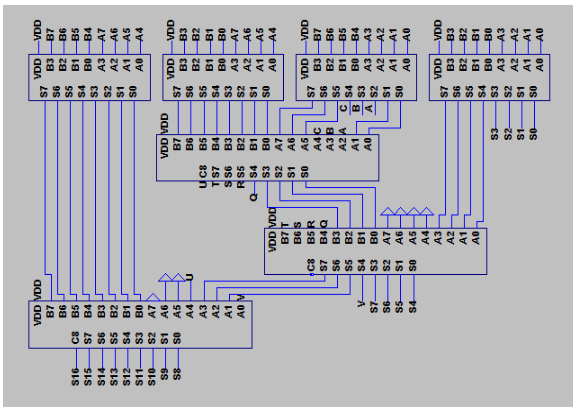


Fig.17. Schematic of 8x8 multiplier

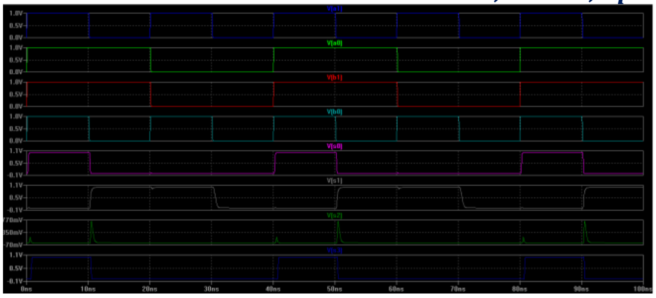


*Fig.18. 2x2 multiplier results using CMOS*

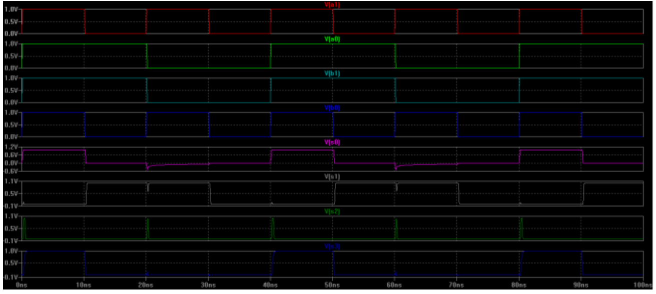


*Fig.19. 2x2 multiplier results using GDI*

## IV. FUTURE WORK AND CONCLUSION

In this paper, a deep detailed study of 8x8 bit Vedic Multiplier is carried out. Multiplier is very important in DSP (Digital Signal Processing) and Math processors so it should be accurate and here tried to make this thing possible.

Table II.
DELAY AND POWER CONSUMPTION IN 8X8 MULTIPLIER

| Technology | VDD | Delay | Average Power Consumption |
|---|---|---|---|
| GDI | 1V | 732.92 ps | 907.12 uW |
| CMOS | 1V | 634.544 ps | 764.32 uW |

The design has been implemented using PTM 45nm GDI technology as well as CMOS at 1.0v supply voltage in LTSpice IV tool. Also CMOS has very low power dissipation compared to GDI Multipliers because in GDI the number of transistors used is more than that used in CMOS. The power consumption of 0.907 mW and a delay of 732.92 ps has been observed for Proposed GDI 8x8 bit Vedic Multiplier. The output waveforms for 2x2 multiplier for both GDI implementation and CMOS using inverter have been shown in Fig.19 and Fig.18 respectively. Fig.19 shows that the output waveforms are better than Fig.18, but this accuracy in result has been obtained at a cost in number of transistors. Thus causing more power consumption than normal GDI implementation. Power and number of transistors are the limiting factors as it is compared with other designs.

The future work of this paper lies to carry out the multiplication of floating point numbers and to increase the number of bits to be multiplied. Furthermore various other implementation techniques like Transmission Gate (TG) or Pass Transistor Logic (PTL) should be implemented for this Vedic Multiplier.

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