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Three Phase Inverter With Reduce Number of Switches

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Abstract — The main objective of this paper is to reduce the number of power electronics components by using the novel topology of multilevel inverter.to reduce number of switches as increased the level of inverter the number of switches should be reduce as per the different calculation of components. In the industrial application on the basis of drives the multilevel inverter can do great job to get desired output. But in the conventional multilevel inverter use of power electronics components are more as compare to unconventional or proposed topology of multilevel inverter. The proposed multilevel inverter use only 16 switches for 5-level and as increased the level the level the number of switches will reduced. As using the novel topology with help of Selective Harmonics Elimination (SHE) technique for give the triggering pulse to the switches. By using this PWM method the lower order harmonics will reduced gradually.

Keywords- Multilevel inverter, new multilevel topology, SHE, proposed topology, MATLAB® Simulink.

I. INTRODUCTION

Multilevel inverters contain number of switching devices and dc voltage supplies, the output of which produces voltages with stepped waveforms. Multilevel technology has started with the three-level converter followed by numerous multilevel converter topologies. Different topologies are available for reduced lower order Harmonics. Multilevel power conversion was first introduced more than two decades ago. The general concept is to utilizing a higher number of power electronics switches to perform the power conversion in small voltage steps. There are many advantages to this approach when compared with the conventional power conversion approach.

The conventional multilevel inverter configurations are neutral point clamped (NPC), the flying capacitor (FC), and the cascaded H-bridge (CHB). But the main disadvantages of this topology are deviating voltage of neutral-point voltage in NPC, the unbalanced voltage in the dc link of FC, and the large number of separated dc supplies in CHB. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Another feature of multilevel inverters is that the semiconductors are wired in a series-type connection, which allows operation at higher voltages. The series connection is create with the help of clamping diodes, which help to eliminates overvoltage concerns. Furthermore, since the switches are not truly series connected, their switching can be staggered, which reduces the switching frequency and thus the switching losses.

One major disadvantage of multilevel power conversion is the higher number of power electronics switches required. It should be indicate that lower voltage rated switches can be used in multilevel converter and, therefore, the active semiconductor cost is not increased when compared with the two level cases. However, each active semiconductor added requires associated gate drive circuits and adds further complexity to the circuit layout. To reduce this types of problems in power conversion use the proposed topology of multilevel inverter with reduced the number of component. By using this topology the switching losses of the inverter will reduced and get better output in the form of stepped wave. For generate the gate pulse to switches use Selective Harmonics Elimination technique used. With the help of this technique reduced the lower order harmonics and get more accurate control output of the multilevel inverter.

II. DETAILS EXPERIMENTAL

2.1. Switching Strategy

The typical configuration of the proposed topology is shown in fig 1.There are three bidirectional switches, two switches-two diodes type, are added to the conventional two level bridge. The main function of these bidirectional switches is to block the higher voltage. A multilevel DC link built by single dc voltage supply with fix magnitude of 4Vdc and cascaded H Bridge having two unequal dc voltage supply of Vdc and 2Vdc are connected with bridge terminal. On the basis of desire number of output voltage level the number of H Bridge cell are used. So proposed inverter is configure to get five voltage level, and we get the power circuit of the H Bridge makes use of two series cell having two unequal dc

voltage supply. In every H bridge cell two switches are turned ON and OFF as per the inverted condition to output with two different voltage level. In the first cell dc voltage supply is added when switch T1 is turned ON and lead to Vmg= +Vdc. At that time if switch T2 turned on Vmg = 0. Likewise, the second H bridge cell dc voltage supply 2Vdc is added when switch T3 is turned ON and Vom= +2Vdc. At that time if switch T4 is turned ON resulting in Vom= 0. By considering the phase A the operating status of the switches are given in the table I.

"Table 1: Switching State Sa and Inverter Line-to-Ground Voltage Vag"

Sa	Q1	S1	S2	Q2	T1	T2	T3	T4	Vag
4	On	Off	Off	Off	On	Off	On	Off	+4Vdc
3	Off	On	On	Off	On	Off	On	Off	+3Vdc
2	Off	On	On	Off	Off	On	On	Off	+2Vdc
1	Off	On	On	Off	On	Off	Off	On	+Vdc
0	Off	Off	Off	On	On	Off	Off	On	0

2.2. Comparison study

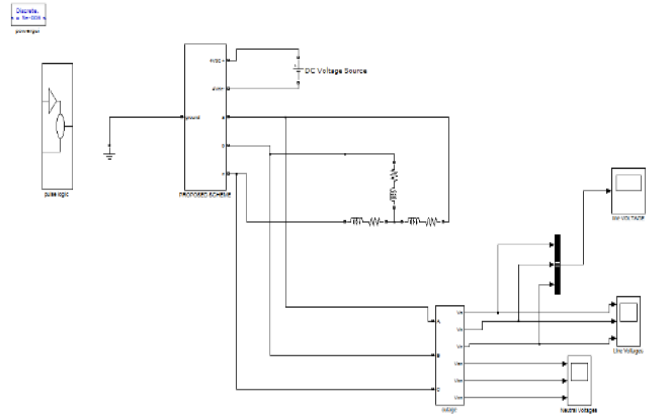
In the comparison study the proposed inverter is compared with different types of multilevel inverters such as NPC, FC, and CHB. As per the earlier study that is suggested that the number of power electronics components is reduced by the use of proposed topology od multilevel inverter as compare to the three conventional multilevel inverters. In the table 2 explain the required number of power electronics components for the proposed N level and also for the conventional topology of multilevel inverter. As per the given data in the table 2 we can calculate the number of components as per the output level of the inverter. It is observed that the inverter employs switching devices with high voltage rating. That results in high cost per-switch. Since the topology is introduced with reduced number of switches, gate driver circuit, diodes and no clamping capacitors are involved, the semiconductor devices expenses are considerably recovered.

"Table 2: Comparison between components of conventional and proposed multilevel"

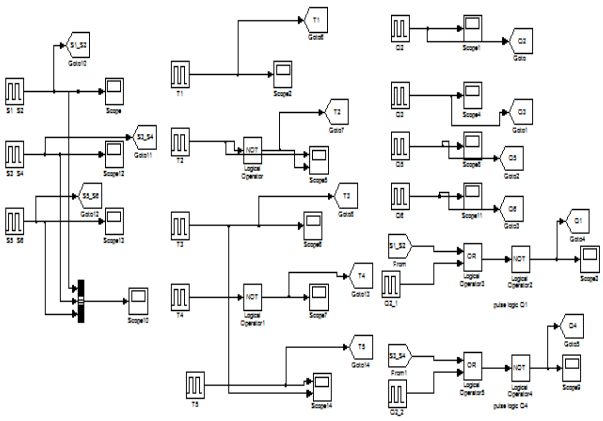
Inverter type	NPC	Flaying capacitor	cascade	Proposed
Main switches	6(N-1)	6(N-1)	6(N-1)	3((N-1)+4)
Main diodes	6(N-1)	6(N-1)	6(N-1)	3((N-1)+4)
Clamping diodes	3(N-1)*(N-2)	0	0	0
DC bus capacitor	(N-1)	(N-1)	3(N-1)/2	(N-1)/2
Flaying capacitor	0	3/2(N-1)*(N-2)	0	0
Total numbers	(N-1)*(3N-1)	1/2(N-1)*(3N+20)	27/2(N-1)	(13N+35)/2

III. MATLAB/SIMULINK Model

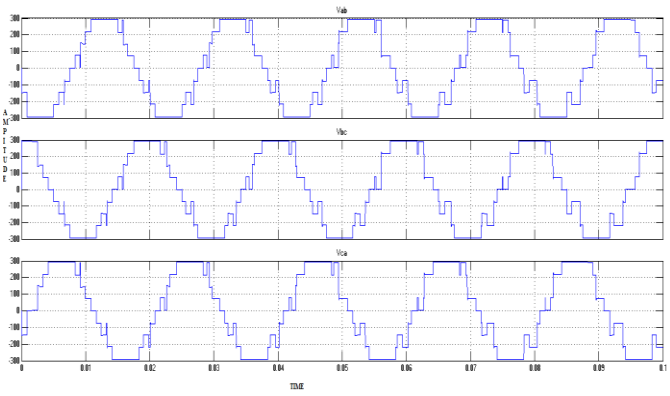
3.1. Proposed topology with RL load



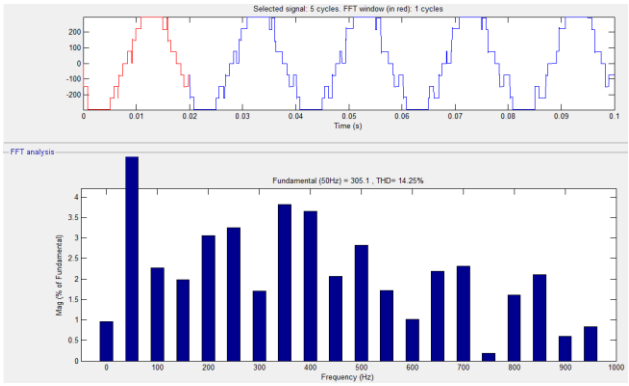
"Figure.1. MATLAB/SIMULINK Model of proposed topology With RL load"



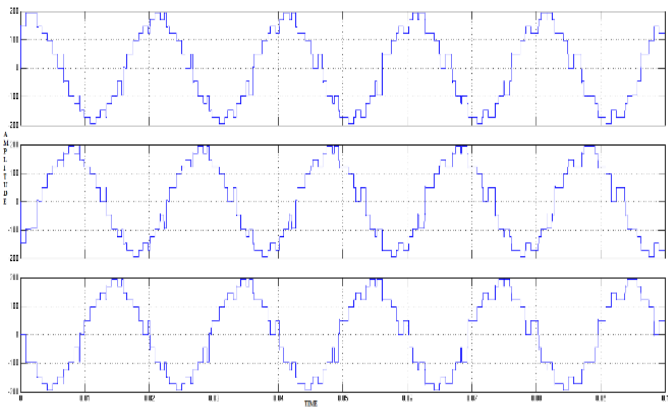
"Figure.2. Pulse Generating Circuit"



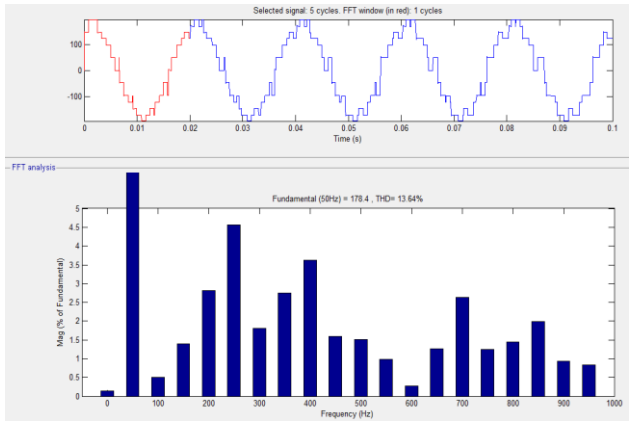
"Figure.3. line voltage"



"Figure.4. FFT Analysis of line voltage"

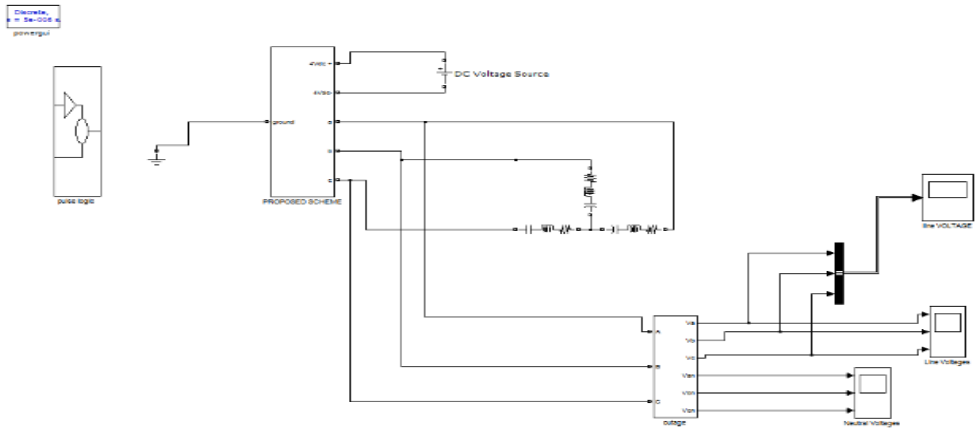


"Figure.5. Neutral voltage"

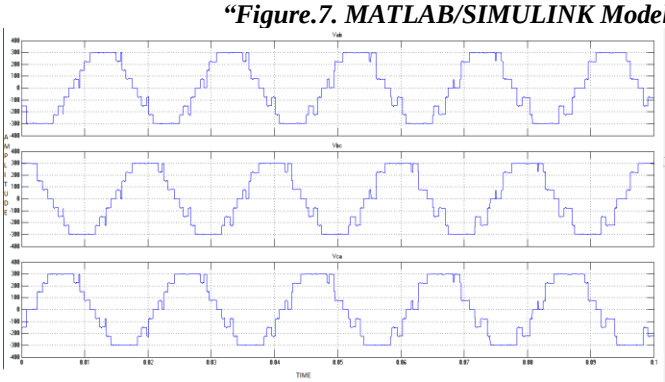


"Figure.6. FFT Analysis of Neutral voltage"

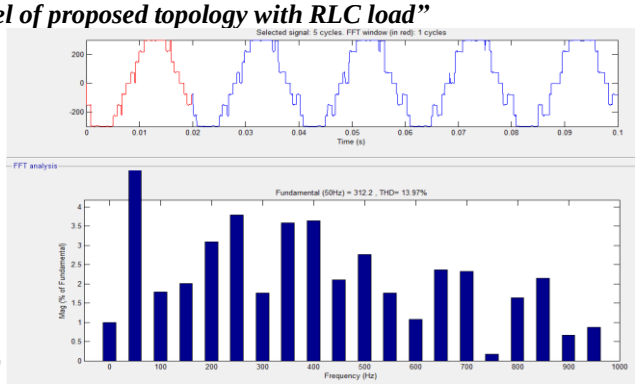
3.3. Proposed topology with RLC load



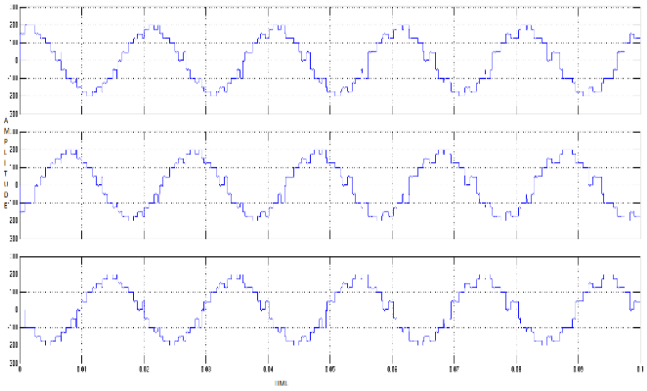
"Figure.7. MATLAB/SIMULINK Model of proposed topology with RLC load"



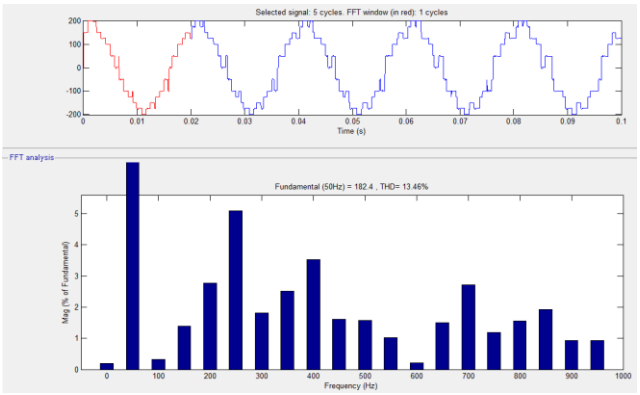
"Figure.8. Line voltage"



"Figure.9. FFT Analysis of line voltage"



"Figure.10. Neutral voltage"



"Figure.11. FFT Analysis of Neutral voltage"

VI. CONCLUSION

By the simulation of conventional topologies of multilevel inverter and proposed topology of multilevel inverter we conclude that the THD% of conventional multilevel inverter is greater than the proposed topology of multilevel inverter. When we simulate the circuits of multilevel inverter with RL and RLC load with different configuration of multilevel inverter we get different ratings of THD% of each topology.

VII. FUTURE ENHANCEMENT

It is shown that this topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc. In the mentioned topology, the switching operation is separated into high- and low-frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype.

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