



Design and Implementation of Hogge Phase Detector using Transmission Gate Logic

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Abstract— Phase detector is the first block of Phase Locked Loop. It is a nonlinear device the output of which contains the phase difference between the two oscillating signals. The advantage in most of the phase detector is that their low frequency response is actually linear over some range rather than sinusoidal. A different view is required in the analysis of digital phase detector from that of classical mixing detectors. The exact behavior of these digital phase detectors should be nonlinear but the low frequency behavior is often linear. The circuit of phase detectors is more important in dealing with specific circuit conditions than to make analysis simpler. The Hogge Phase Detector using Transmission Gate Logic in 45nm CMOS technology is implemented here in LTSpice IV tool because of its small output jitter and self-correcting ability and linearity.

Keywords: Phase Detectors, Hogge Phase Detectors, Transmission Gate Logic, Timing Diagrams, Simulation Results

I. INTRODUCTION

In this paper a description of phase detectors along with design and implementation of Hogge phase detector using Transmission Gate Logic is presented. Linear and nonlinear phase detectors have been described widely uptill now. Most of the commonly used phase detectors have sequential elements in them. Some of the linear phase detectors do not use sequential elements. To work for random NRZ Data, a linear phase detector is proposed which is known as hogge phase detector named after its inventor C.R.Hogge. It contains two D-flip flops and two XOR gates for its operation. As flip flops generally goes into metastable regions, it is however speed limited. It uses non sequential elements. It generates a reference and difference pulse at every data transition. It also has the self-correcting ability.

II. PHASE DETECTORS

In PLL designs, many different types of phase detectors have been used. Broadly, they can be classified into two categories:

- Multiplier Circuits
- Sequential Circuits

Useful DC error output is generated by multipliers as the average product of the input signal waveform times the local oscillator waveform. An output voltage that is generated by a sequential phase detector is a function of the time interval between a zero crossing on the signal and a zero crossing on the VCO waveforms. The main advantage of sequential phase detector is that it is capable of detecting both the frequency and phase differences. Sequential phase detectors are built up from digital circuits and operate with the help of binary, rectangular input waveforms.

Specifications of a Phase Detector:

- DC offset
- Maximum DC output(DC output occurring with in-phase signals)
- Isolation between ports
- Polarity of output voltage
- Frequency response (Variation of maximum DC output with input frequency)
- Temperature variation of DC offset

Applications of Phase Detectors:

Phase detectors are used in

- Phase Locked Loop(PLL)
- Radar and Telecommunication System
- Motor Control
- Demodulators
- Servo Mechanism

Classification of Phase Detectors:

Three main digital phase detectors are

- XOR phase detector
- Hogge phase detector
- Bang Bang or Alexander phase detectors

III. HOGGE PHASE DETECTOR

To recover the random NRZ data, the most commonly used linear phase detector is Hogge Phase Detector shown in figure 1.

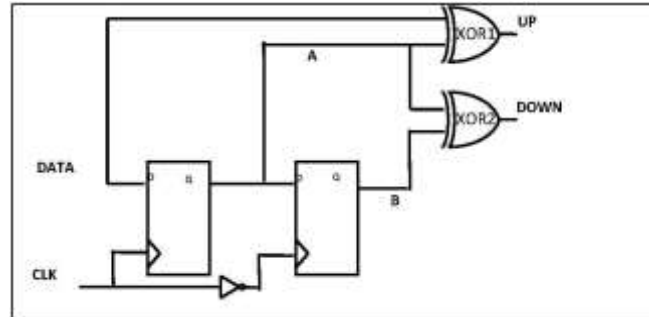


Figure 1. Hogge Phase Detector

The two pulses that come out of the XOR gates are essentially subtracted by the hogge phase detector. This subtraction is accomplished by the charge pump. The gate XOR1 generates a reference pulse. This reference pulse is exactly half a bit time in width. The width of the pulse generated by XOR2 gate depends on the phase error between the edges of Data and edges of CLK. When the phase difference between CLK and Data is half a bit, a very little charge in the PD output is generated as both those pulses cancel each other. The reason behind this little charge that is generated in the phase detector output is because of the UP and DOWN pulses are not generated simultaneously.

The linear characteristics of the above mentioned Hogge phase detector is shown in the figure 2.

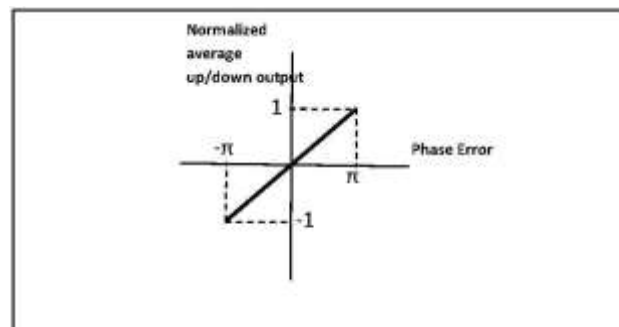


Figure 2. Linear characteristics of Hogge phase detector

The net pulse width at the output is linearly proportional to the phase difference between the center of Data and the edges of CLK which results in Linearity. The shape of the transfer function is like a saw-tooth. This is due to the phase being a modulo- 2π quantity. The slope of the transfer function when the phase error is close to zero is defined as the phase detector gain (KPD).

There is a phenomena called dead zones in the Linear Phase Detectors. The state in which there is no activity on the control lines when the phase error is close to zero is defined as Dead Zones. The inability of digital gates to generate infinitely small pulses is the main reason for the dead zones to arise.

The Hogge phase detector under lock conditions is shown in the timing diagram of figure 3.

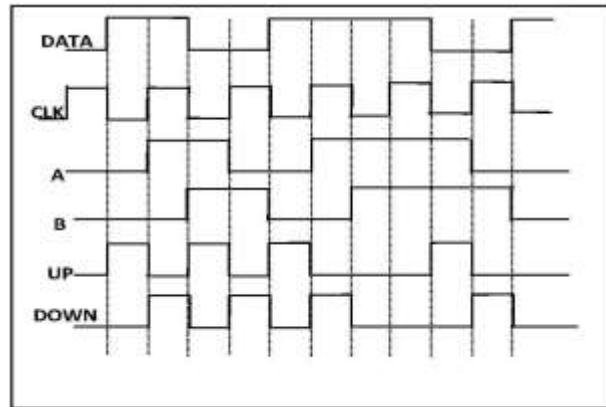


Figure 3. Timing diagram of hogge phase detector under lock conditions

The timing diagram of hogge phase detector when the Data leads CLK is shown in figure 4.

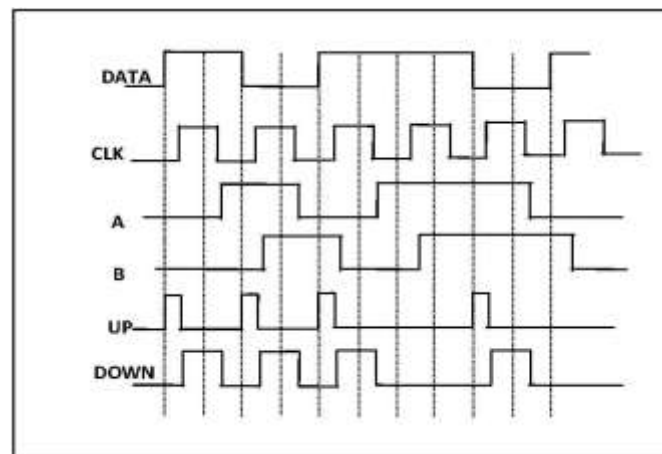


Figure 4. Timing diagram of Hogge phase detector when Data leads CLK

The timing diagram of hogge phase detector when the Data lags CLK is shown in figure 5.

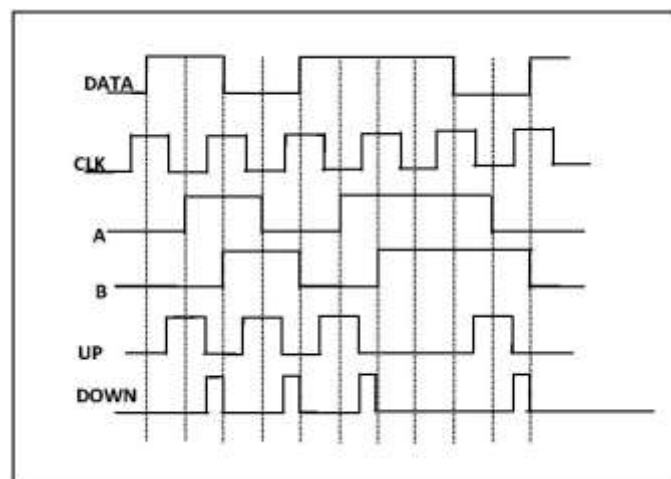


Figure 5. Timing diagram of Hogge phase detector when Data lags CLK

Limitations of Hogge phase detector:

As we know that Hogge phase detector has a very small jitter generation, it still presents some limitations due to the phase detector itself compared with binary phase detector.

- The gain of the Hogge phase detector is sensitive to incoming data transition density. Assume the incoming data pattern changes from 010101... to 001100110011..., the phase detector gain will be reduced by half.

- The bandwidth requirements of the Hogge phase detector is limited. Such as it is difficult to design a Hogge phase detector for the applications which require 10Gb/s bandwidth.
- Static phase offset will be caused due to the mismatch between the D flip flops in the circuits and thus affects the jitter performance of the CDR circuits.

Due to the above mentioned limitations, Hogge phase detector is generally not used for 10Gb/s CDR design.

IV. LOGICS USED IN PHASE DETECTORS

The most basic element used in any of the phase detectors is D flip flop. This D flip flop can be made using following five different kinds of logics.

- Transmission Gate Logic
- TSPC Logic
- Domino Logic
- GDI Logic
- CMOS Logic

Thus by using D flip flop with five different types of logics, we get Hogge phase detector with five different types of logics.

In this research paper we have explained only the Transmission Gate Logic as we get the nearest output as compared to the ideal output of the Hogge phase detector by using this particular logic.

Transmission Gate Logic:

In this logic, a transmission gate is made up of two field effect transistors. In this logic, in contrast to traditional discrete field effect transistors – the substrate terminal is not internally connected to the source terminal. The two transistors, a p-channel MOSFET and an n-channel MOSFET are connected in parallel with this transmission gate. Here only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other via a NOT gate i.e inverter, to form the control terminal.

As with discrete transistors, the substrate terminal is connected to the source connection, so there is a transistor to the parallel diode(body diode), whereby the transistor passes backwards. However, a transmission gate must block flow in either direction. To ensure that the substrate diode is always operated in the reverse direction, the substrate terminals are connected to the respective supply voltage potential. The substrate terminal of the p-channel MOSFET is thus connected to the positive supply voltage potential and the substrate terminal of the n-channel MOSFET connected to the negative supply voltage potential.

V. D FLIP FLOP AND HOGGE PHASE DETECTOR SCHEMATIC AND SIMULATION

The schematic and its simulation are done in LTSpice IV tool. The schematic of D flip flop using transmission gate logic is shown in figure 6.

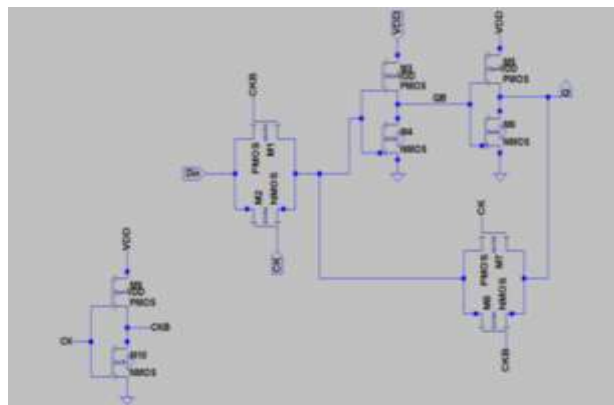


Figure 6. D flip flop using Transmission Gate Logic

The schematic of Hogge phase detector using D flip flop with transmission gate logic is shown in figure 7.

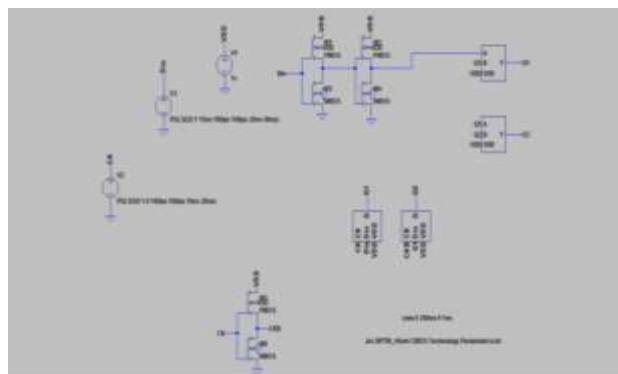


Figure 7. Hogge phase detector with transmission gate logic

The simulation result of Hogge phase detector with transmission gate logic is shown in figure 8.

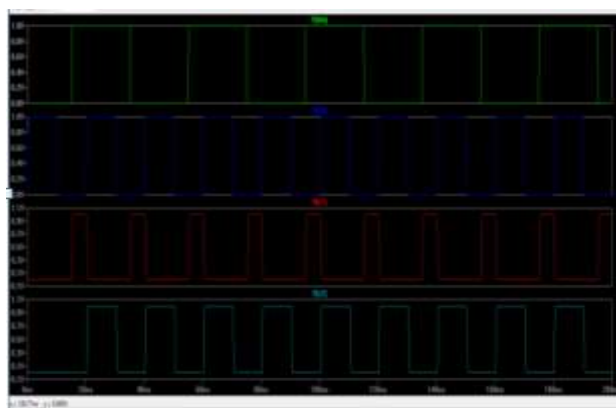


Figure 8. Simulation result of Hogge phase detector

VI. CONCLUSION

In this paper, we can see that using D flip flop with Transmission Gate Logic, a Hogge phase detector can be designed. By comparing simulation results of the designed Hogge phase detector with the ideal outputs, we can conclude that it is possible to design and implement the Hogge phase detector in the 45nm technology with the same output as the ideal ones. We can also conclude that to make this phase detector with any other above mentioned logics, the circuit of the D flip flop with that particular logic must require some design improvements.

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