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Wideband Low Noise Amplifier for Next Generation Wireless RF Frontend: A Review Paper

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Abstract

The volatile growth of the wireless industry, global access to the internet, and the ever increasing demand for high speed data communication are encourage us toward rapid developments in communication technology. Wireless communication plays an essential role in this transformation to the next generation of communication systems. Next generation wireless terminal should support multiple communication standards with different modulation scheme require wideband Radio Frequency (RF) frontend having high gain, low noise figure (NF), good linearity and low power consumption. This can be done using software define radio (SDR) architecture. In SDR architecture of receiver Low Noise Amplifier (LNA) is essential part. In this paper we done meticulous survey of wideband LNA topologies published in open literature suitable for SDR. Measured results of the sample LNA designs from each category are tabulated and discussed with emphasis on gain, NF, input matching, power consumption, and linearity tradeoffs. At the end discuss design challenges of next generation RF frontend wideband LNA.

Keywords- *LNA; Next Generation Wireless Receiver; RF Frontend; SDR; Wideband;*

I. INTRODUCTION

Today's wireless mobile terminal should support multiple communication standards like: GSM, UMTS, WiMAX, LTE, ZigBee, Bluetooth, IEEE 802.11a/b/g etc; operated on difference frequency band and different modulation scheme [1]. This mobile terminal is termed as commercial Software Defined Radio(SDR), as proposed by Mitiola [2].

The ideal SDR architecture proposed by Mitiola (Figure 1) puts very tough requirements on the dynamic range, speed, noise performance and linearity of A/D converter. A practical SDR architecture as shown in figure 2. An LNA relaxes the noise performance and dynamic range requirements while the mixer block reduces the speed requirements of the A/D converter by converting RF signal to IF signal. That is why Low Noise amplifier is essential part in wideband RF Frontend design.

Moreover, the user expectations are major drivers to determine upper bound on power consumption and cost metrics. The new portable wireless products cannot be sold in the market if their battery backup time is shorter. The same principle rules the cost and budgeting paradigm. Thus, future LNAs should have power consumption, gain and NF close to what is offered by state-of-the- art narrowband LNA designs. The bandwidth should be more than 6 GHz to cover all the deployed commercial and upcoming 4G standards.

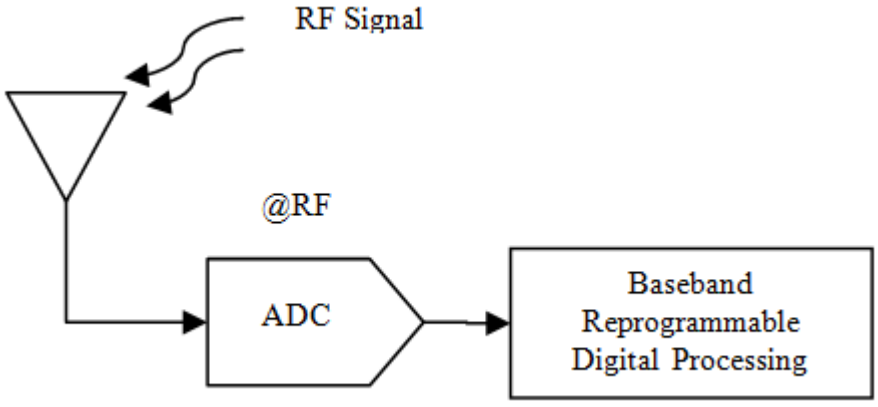

Figure 1. Ideal SDR Receiver.

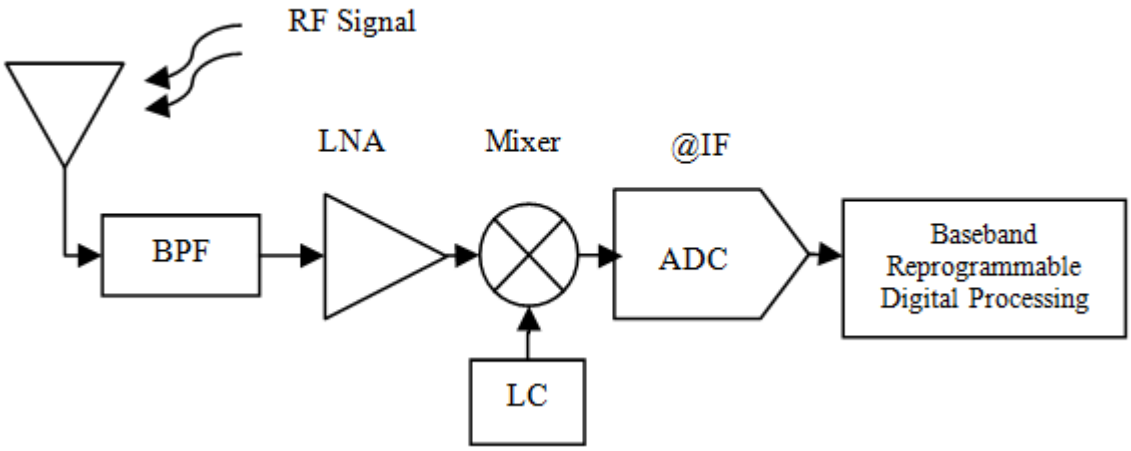

Figure 2. Practical SDR receiver.

II. CHALLENGES IN WIDEBAND LNA DESIGN

In [8], the gain, NF and linearity requirements of a single LNA accommodating GSM, UMTS and WLAN are specified as 23dB, 3 dB and 0dBm respectively. Addition of new standards like WiMAX and LTE will make the LNA specifications even more challenging. Moreover, multiple filters are used at the LNA input to remove blockers.

The linearity parameters of the LNA will become more stringent if these filter specifications are relaxed. This clearly shows that the implementation of a receiver chain without an LNA is practically impossible. In a receiver, the first amplifying block is LNA. Its noise performance defines the NF of complete receiver. A classical narrowband LNA should have high gain, low NF, good linearity, low power, 50 Ω matching and stability at the frequency of interest. To accommodate different standards with different modulation scheme require specification of wideband LNA are:

- Minimum signal reflection by achieving good (50 Ω) input matching (S11⩽–15dB)for all frequencies [6].
- NF⩽3.5 dB over the entire bandwidth [7].
- Higher linearity (IIP3⩾0 dBm) [8].
- Flat gain across the entire bandwidth.
- Unconditional stability over entire frequency range.

III. WIDEBAND LNA TOPOLOGIES

The major challenges of a wideband LNA design can be summarized in terms of S parameters and NF as follows: [24] you.

- Forward gain degradation (decreases in S21) which necessitates some techniques to compensate the gain roll-off.
- Frequency variations of S11 and S22.
- Increase in |*S12*| which will reduce the forward gain and increase the possibility of oscillation and instability.
- NF degradation at high frequencies.

To address these challenges in the design of a wideband LNA, several topologies and circuit techniques have been proposed in the literature. In This section, we will introduce briefly some of the popular wideband architectures and briefly discuss their advantages and disadvantages.

A. Common source with resistive termination:

One good approach to achieve wideband impedance matching is by adding a 50Ω shunt resistor at the input of common source LNA as shown in Figure 3[3]. This topology results in severe tradeoff between NF optimization and input impedance matching. The placement of shunt resistor before the transistor not only attenuates the signal but also add thermal noise. The minimum NF of this approach is [3].

$$NF = 1 + \frac{R_s}{R_I} + \frac{\gamma R_s}{g_m}\left(\frac{1}{R_s} + \frac{1}{R_I}\right)^2 + \gamma g_m R_s \frac{\omega^2}{\omega_T^2} \qquad (1)$$

where γ is a noise parameter and α is the ratio of transistor's transconductance (gm) to drain-source conductance (gds) at zero bias. ω_T is the unity gain crossover frequency.

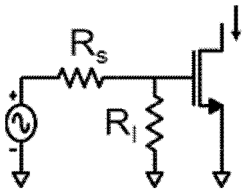

Figure 3. Common source with resistive termination.

B. Comman Gate

In common gate input impedance is 1/gm which is inversely propos anal to transconductance of device. To match

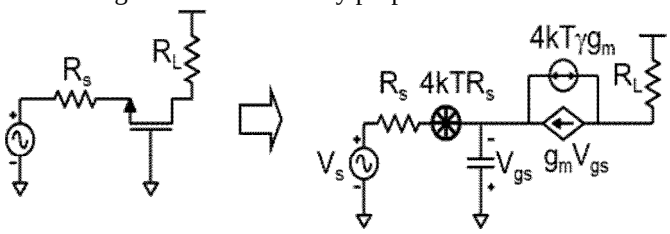

Figure 4. Common gate and its small signal euivalent circuit.

Input admittance Yin=gm+sCgs at lower frequency inout impedance Zin=1/gm. Noise performance of CG structure can be calculated as

$$G_{eff} = \frac{I_{out}}{V_s} = \frac{-g_m}{1 + g_m R_s + s R_s C_{gs}} \qquad (2)$$

$$G = \left|G_{eff}\right|^2 = \frac{g_m^2}{(1 + g_m R_s)^2 + \omega^2 (R_s C_{gs})^2} \qquad (3)$$

$$NF = \frac{N_{device} + G \cdot N_{in}}{G \cdot N_{in}} = 1 + \frac{4kT\gamma g_m}{4kTR_s \dfrac{g_m^2}{(1 + g_m R_s)^2 + \omega^2 (R_s C_{gs})^2}}$$

$$= 1 + \frac{\gamma}{R_s g_m}\left[(1 + g_m R_s)^2 + \omega^2 R_s^2 C_{gs}^2\right]$$

$$= 1 + 4\gamma + \gamma \frac{\omega^2}{\omega_T^2} \qquad (4)$$

Power Transfer of CG Structure

$R_s = R_L = R = 50$ ohm

$$S_{11} = \frac{Z_{in} - Z_s^*}{Z_{in} + Z_s} = \frac{1 - g_m R_s - s R_s C_{gs}}{1 + g_m R_s + s R_s C_{gs}}$$

$$= \frac{-sR_s C_{gs}}{2 + sR_s C_{gs}} \qquad (5)$$

$$S_{21} = 2R_L G_{eff} = \frac{2R_L g_m}{1 + g_m R_s + s R_s C_{gs}}$$

$$= \frac{2}{2 + sC_{gs}} \qquad (6)$$

$S_{11}=0$, $S_{21}=1$ @ Low frequency

NF is low due to no extra resistive noise source as well as NF is independent of power consumption.

In [40] used Common Gate with current reuse Common Source next stage to enhance gain and achieved good gain 14.9dB at power consumption is only 3.4mW in 2.4-11.2GHz band.

C. Negative Feedback Wideband LNA

The classical approach to satisfy the required impedance matching at the input of a wideband LNA is to employ negative feedback. This technique will provide a flat gain and reduces the sensitivity of the circuit to the MOS device parameters. The feedback circuitry may increase the minimum *NF* and reduce the maximum achievable gain.

Different topologies of negative feedback amplifier exist in the literature. One of the most popular variations of negative amplifier is the shunt-series amplifier, symbolically shown in figure 5.

To achieve wideband input and output matching, one should design for zero *s11* and *s22* after finding the S parameter expressions for this network. Solving for *s11=s22=0*, yields the following equation that relates the values of *R1* and *R2* [9]:

$$R_2 = \frac{g_2^2}{R_1} - \frac{1}{g_m} \qquad (7)$$

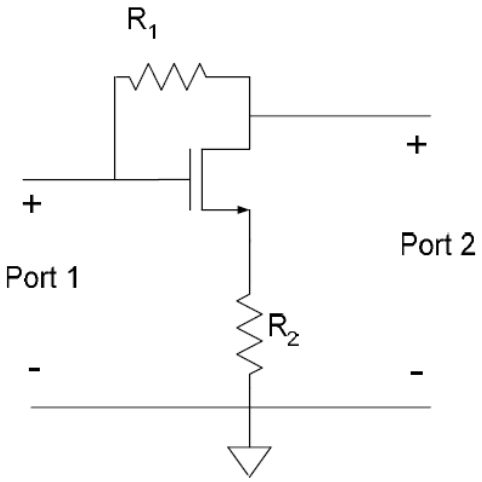

Figure 5. Two port model of a shunt-series amplifier [48]

An appropriate choice of R1 and R2 values will satisfy (7) and hence the input and output matching. It will also result in a flat in-band forward gain with no dependency on the MOS device parameters ([9]). However, (7) is only valid in low frequencies where all parasitic effects may be ignored. In gigahertz applications parasitic capacitances and inductances become non-negligible and the power gain starts to roll-off. The input and output matching also degrades significantly in high frequencies.

One implementation of a negative feedback amplifier is shown in figure 6. In this circuit [10] the input stage is a common source amplifier and the feedback stage is a common drain amplifier. A simple analysis of this circuit shows that gm,M_2 of the common drain stage controls the input impedance, while gm,M_1 of the common source amplifier contributes to the gain and *NF* of the overall LNA. This is in contrast to the *1/gm* termination architecture where the *gm* of the input transistor is set by the input matching requirements and leaves no freedom for *NF* optimization. The main disadvantage of this architecture is the relatively high power consumption due to the addition of the feedback stage.

In another work, negative feedback is employed to realize a UWB LNA covering a 7GHz bandwidth (2 – 9 GHz) [11]. The schematic of this LNA is shown in figure 7. The input stage adopts a shunt-series feedback structure to satisfy the wideband input matching. The inverter configuration at the input is to increase the total trans-conductance (gm1+gm2), and hence the open-loop voltage gain for a fixed power consumption.

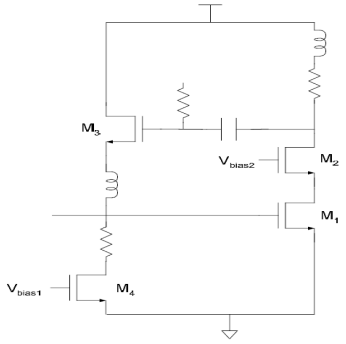

Figure 6. Common drain feedback LNA [48]

The increase in the total transconductance also allows for a higher shunt resistor for a given 3dB bandwidth. This increase in the value of shunt resistance will lend itself to a lower total NF. Two degeneration inductances Ls1 and Ls2 are used to partially cancel the parasitic capacitances at the input of the LNA, which would otherwise devastate the impedance matching at high frequencies. The second stage is a simple cascode amplifier with a shunt-peaking load that provides the required gain of the entire LNA [48].

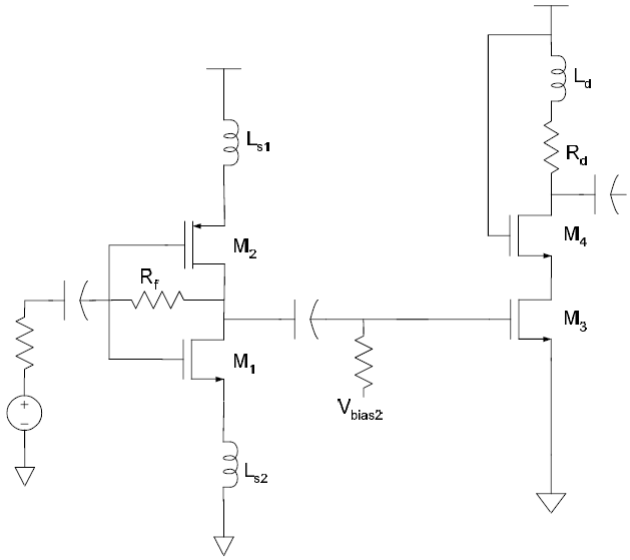

Figure 7. Two-stage LNA for UWB applications [48]

Negative feedback amplifiers may also be used as the second stage of wideband amplifiers. One example is the work in [12] that combines the benefits of 1/gm termination with those of the negative feedback amplifier. Figure 8 depicts the schematic of this architecture. The input stage uses a common-gate amplifier to achieve 50Ω impedance matching. However, this matching sets the value of gm,M_1, and another stage is required to provide sufficient gain over the entire band-width. This second stage is realized by employing M_2 in a shunt-feedback configuration. One drawback of this feedback is that the degradation of forward gain at high frequencies causes a positive feedback through Rf., thus leading to oscillation at the output. To alleviate this problem, L_f is connected in series with the shunt resistor, Rf. This will reduce the feedback at high frequencies and also improve the gain flatness. L_{d1} and L_{d2} are inductive loads to compensate the gain degradation at high frequencies[48].

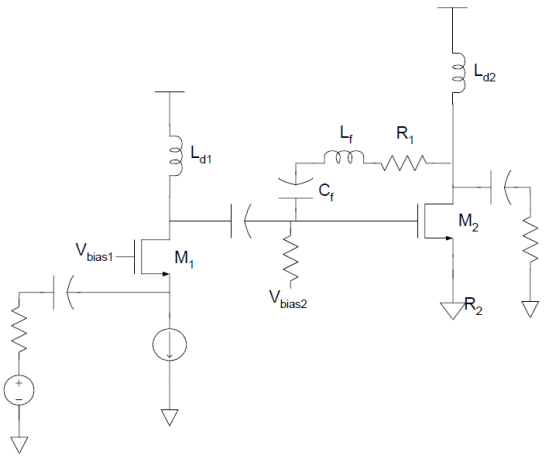

Figure 8. Two stage wideband LNA for UWB applications [48]

In [12], a UWB LNA is successfully designed and simulated using this two-stage architecture.

The Common Gate (CG) LNA is good solution of wideband input matching. Also, CG LNA have good linearity, stability and low power consumption. However its main drawback is the relatively high NF and low gain due to input impendence matching need to restrict value of trans-conductance. Different negative feedback techniques are used in CG LNA like capacitive cross coupling, dual negative feedback, and positive –negative feedback to overcome tradeoff between input impendence matching and the NF, which lead to simultaneous reduction in noise and power dissipation. In

[39] authors have proposed inductorless multiple feedback paths CG LNA and achieve 1.85dB minimum NF, 23dB Gain with good linearity (IIP3=-2.3dBm) at a low power dissipation (2.8mW) in 0.1-1.77GHz band. In [41] proposed pseudo-differential resistive feedback wideband LNA with noise and distortion cancellation.

In [42] proposed linearization techniques for wideband LNA by using inverter topology with resistive feedback in first stage to provide high linearity and cascode amplifier with shunt series inductive peaking to extend bandwidth and achieve high gain simultaneously in second stage. The proposed [42] wideband LNA achieve good linearity +6.4dBm IIP3, 15dB gain, 3.5dB minimum noise figure and 16.2mW power consumption in entire 3.1 -10.6GHz band.

The aforementioned trade-offs among power, bandwidth, and gain are a serious drawback of any feedback system. For illustration purposes, consider the conceptual schematic of a shunt feedback amplifier as shown in figure 9. The input impedance is given by $Zin(s)=Rs/(1+sRsCin)$,where Rf and A are chosen in a way that $Rf/(1+A)=Rs$. In order to achieve input matching at 10GHz, i.e., $|\Gamma|<-10$dB, the input capacitance (Cin) is limited to as low as 200fF [13]. This limits the width of the input transistor and hence the maximum gain of this stage. To overcome this problem, most of the feedback amplifiers must include a second stage to boost the gain. Two stages of gain directly translate into higher power consumption, which is not a desirable outcome[48].

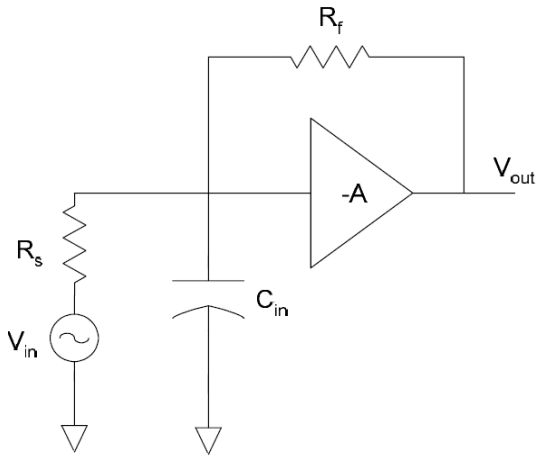

Figure 9. Simplified block diagram of a shunt-feedback LNA [48]

D. Thermal-noise-cancelled Wideband LNA

Feedback amplifiers, as discussed earlier, typically require two stages of amplification in order to provide sufficient gain and thus dissipate a large amount of power. Also note that the input impedance in a feedback amplifier is a function of the amplifier gain. However, this dependency is not straightforward, and the impedance matching is susceptible to the variations of the gain.

To overcome these shortcomings, [14] suggests the use of a noise-cancelling feed-forward technique that decouples noise and input matching requirements. The conceptual schematic of this LNA is shown in figure 10. The noise current of the amplifier, In,i flows out of the MOS device and passes through R and Rs. Therefore, the instant noise voltages at nodes X and Y have the same polarity. Conversely, the signals at X and Y are of opposite polarities, simply due to the negative gain of the amplifier. This difference between the sign of signal and noise suggest the possibility of cancelling the noise while boosting the signal up.

To do so, another gain stage is inserted between the first stage and the output. The voltage at node Y (signal plus noise) is added with the properly scaled negative replica of the voltage at node X (the block shown by $-Av$ generate this replica)[15]. By the proper choice of Av, the noise contribution of the MOS device becomes equal to zero, and a low NF can be obtained over a wide range of frequency. The analysis in [15] derives the appropriate value of Av in terms of circuit elements R and Rs:

$$A_v = 1 + \frac{R}{R_s} \qquad (8)$$

It is also shown that, under these conditions, the noise contribution of different components is as follows:

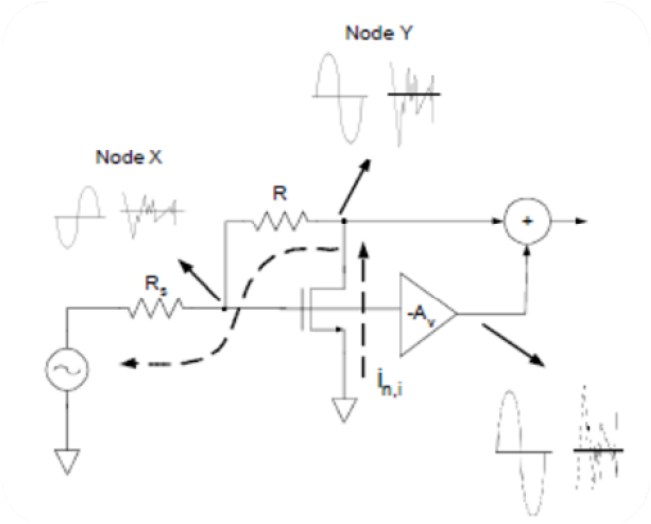

Figure 10. Schematic of thermal noise cancelling technique [48]

The idea of noise cancellation can be extended to any type of amplifier that has 1) a stage of impedance matching, 2) an auxiliary amplifier for sensing the voltage across a real input source, and 3) a circuit to combine the output of two amplifiers to cancel out the noise of the impedance matching stage. Some implementations of this idea are proposed in the same paper[48].

Despite all these benefits, the dominant pole at the input (node X) may limit the bandwidth at high frequencies. Furthermore, due to the existence of the parasitic capacitances, *NF* increases quadratically with the frequency. These effects, along with the high power consumption required by the two amplifiers, may limit the applications of this architecture.

Wideband noise cancelling LNAs reported in literature consume very large power because of the addition stages require for noise cancelling. This make them inappropriate for portable applications. In [46] authors have proposed novel current reuse LNA with noise cancelling technique. And achieve 9.97mW power consumption with gain 10.3dB, NF 3.68dB in entire 2.35-9.37GHz band.

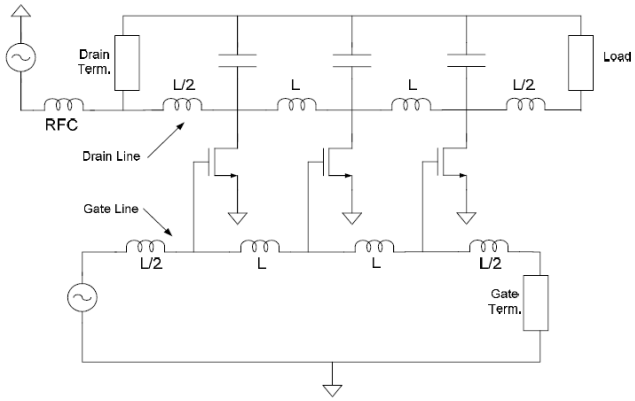

Figure 11. Schematic of a basic distributed amplifier [48]

E. Distributed Amplifier

Distributed amplifiers (DA) (also known as travelling wave amplifiers) employ an architecture in which several active devices are connected in parallel [17]. A basic distributed amplifier is shown in figure 11. The output current of individual amplifiers combine in an additive fashion, and this dictates a relatively low gain for this architecture. The advantage of this architecture comes from the fact that the input capacitances of these amplifiers are distributed in an LC network which allows for the realization of amplifiers with large bandwidths. In fact, the series inductive elements and capacitances of MOS devices form an artificial transmission line, which allows the flow of the signal to the end of the gate line. The signal fed to the gate of the MOS device is transferred to the drain line through the trans-conductance (gm) of the device. If the phase velocity on the gate and drain lines are identical, then the signals at the output add in the forward direction as they arrive at the output. Many wideband LNAs in CMOS have been realized using DA architectures [18][19]. However, the large power consumption of this architecture is a major drawback and makes it unsuitable for low-power portable systems.

These architectures are the most well-known works in the literature of wideband LNA design. Although successfully implemented for some applications, there are still many issues that need to be addressed when it comes to the design of highly integrated LNAs. For instance, the large power consumption of most of these architectures is a major problem, which may eliminate the feasibility of their integration for low-power multi-standard applications. Moreover, a well established methodology is needed to provide the general guidelines for the design of wideband and multi-standard LNAs [48].

IV. CONCLUSION

In this paper, we have presented a rigorous study of different types wideband LNAs published in open literature. Most of all published topologies of wideband LNA used CMOS technology of choice for future commercial RFICs due to its supreme integration capability and extremely low cost per transistor. Here comparison of wideband LNAs done based on its circuit topologies used instead of the technology node used for manufacturing. The main purpose of this review is to find potential circuit topologies suitable for future wireless RF Frontend wideband LNAs. The LNAs are one of the major hurdles and their successful realization will pave the way to commercial SDR.

A simple link budget spreadsheet of today's majority standards shows that linearity is the most exigent requirement as posed by the legacy of GSM standard (0dBmblocker). Therefore, P1dB of higher than 0dBm has proved to be the toughest requirement on multi-standard LNAs. None of the LNAs reported so far meet the requirements of NF, gain, impedance matching, power consumption and linearity simultaneously. There are several reported designs which come close to achieving these specifications except for linearity (P1dB, IIP2, and IIP3) requirements. If we take a closer look, we realize that the linearity requirements (P1dB 0 dBm) along with gain 10dB cannot be met in50 Ω impedance matched circuits implemented in nanometer CMOS. This linearity-gain tradeoff becomes more stringent as the power supply scales down in latest technology nodes. As the P1dB or IIP3 cannot exceed supply voltage, hence better linearity with recent nodes is a major limitation in existing LNA designs.

TABLE I. LITERATURE SURVEY OF WIDEBAND LOW NOISE AMPLIFIER

Source	CMOS Technology (um)	BW (GHz)	S21 (dB)	NF (dB)	IIP3 (dBm)	Power Consumption (mW)	Topology
JSSC-2004 [20]	0.25	0.002-1.6	13.7	2.4	0	35	R FB +NMOS/PMOS
JSSC-2004 [21]	0.18	2.3-9.2	9.3	4	-6.7	9	CS + degeneration and input BPF
JSSC-2005 [22]	0.18	2-4.6	9.8	2.3	-7	12.6	CS + series RC FB
ICAT-2005 [23]	0.18	2.7-9.3	10	3.3	-0.3	14	Cascode + input HPF
JSSE-2006 [24]	0.18	3.1-10.6	9.5	5-5.6	-13	9.4	Cascode + input filter
JSSCC-2006 [25]	0.18	3-5	<16	2.2	-9	7.68	CS + miller effect input matching filter
JSSC-2006 [26]	0.18	0.04-7	8.6	4.2	+3	9	Distributed cascode
JSSC-2007 [27]	0.13	3.1-10.6	15.1	2.5	-8.5	9	CS + reactive FB
JSSC-2007 [28]	0.18	1.2-11.9	9.7	4.7	-6.2	20	CG + noise cancellation
JSSC-2007 [29]	0.18 SiGe	0.1-11	8	2.9	-3.55	21.6	Distributed cascode + BW enhancement
ISSCC-2007 [30]	0.13	1-7	17	2.4	-4.1	25	Cascode + CD FB
JSSC-2008 [31]	0.13	0.8-2	14.5	2.6	16	17.4	CG + noise and distortion cancellation
MJ-2008 [32]	0.18	5-6	20.5	1.8-2.6	-6.2	2	Cascode + inter stage LC network
ISSCC-2009 [33]	0.18	0.3-0.92	21	2	-3.2	3.6	Differential CG + C Cross coupling
ISSCC-2009 [34]	0.13	3.1-10.6	15	<4.5	-12.5	26	Weighted distributed cascode
TCAS-II -2010 [35]	0.18	3.1-10.6	13.9	4.7	-8.5	14.4	Parallel RC FB
MTT-s 2010 [36]	0.09	3.1-10.6	10.5	3.2	4	21.6	Cs + Π input filter
MTT-S 2010 [37]	0.18	31.-10.6	13	4.68	-12	10.34	CS + RLC input filter
RFIC 2010 [38]	0.09	21	15.4	6	-6.6	12.5	Distributed CS + tapered transmission line
MTT-2011 [39]	0.09	0.01-1.77	23	2	-2.85	2.8	Differential CG + multiple feedback
IET MAP 2012 [40]	0.18	2.4-11.2	14.8	3.9	-11.5	3.4	CG + current reuse
MTT-2012 [41]	0.13	0.6-3	42	3	-14	30	Pseudo differential + resistive FB
IJEC-2012 [42]	0.18	3.1-10.6	15	3.5-3.9	6.4	16.2	Inverter with FB
MWCL-2012 [43]	0.065	0.01-2.8	32	1	-13.6	40	Cascode + active –C element
TCAS-II-2013 [44]	0.18	0-1.3	10	3	+7.5	18	Cascode + active feedback
IJMST-2013 [45]	0.18	2.5-16	11	3.3	-	20	RC FB CS + current reuse
IJEC-2015 [46]	0.13	2.35-9.37	10.3	3.68	-4	9.97	CG current resue + noise cancelling
MJ-2015[47]	0.13	3.5-5	14	3.5-3.9	4	21	Fully differential + active FB + Noise cancelling

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