IMPLEMENTATION AND COMPARITIVE STUDY OF VEDIC MULTIPLIERS WITH DIFFERENT ADDERS USING URDHVA-TIRYAKBHYAM SUTRA

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Abstract

Multiplier is the vital component and key block in high speed processor or computing machine like ALU,MAC,DSP,FFTs,etc. With the increasing constrains on delay, more emphasis is being laid on design of faster multiplications. To enhance speed many modifications over the standard modified booth algorithm, Wallace tree methods for multiplier design have been made.Amongest these Vedic multipliers based on Vedic mathematics are presently under focus due to these being one of the fastest and low power multiplier. There are sixteen sutras in Vedic multiplication in which Urdhva- Tiryakbhyam has been noticed to be the most efficient one in terms of speed. I n this paper design and implementation of 64x64 Vedic multiplier is described. It has been modified with different adders and performance is compared in terms of propagation delay. It is proved that Vedic multiplier with simple adder achieves minimum propagation delay.

Keywords *-Multiplier; Vedic Multiplier; Vedic Mathematics; Adders; Urdhva-Tiryakbhyam Sutra*

I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation-Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution ,Fast Fourier Transform(FFT),filtering and in microprocessors in its Arithmetic And Logic unit(ALU).Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications.

Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signals and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier with reduced delay

II. VEDIC MATHEMATICS

The word "Vedic" is derived from the word Veda which means the store-house of all knowledge. Vedic mathematics is part of four Vedas (books of wisdom). Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja(1884-1960) rediscovered Vedic Mathematics.Swamiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae).Vedic mathematics is mainly based on 16 Sutras. The advantage of Vedic mathematics lies in the fact that it reduces the cumbersome-looking calculations in conventional mathematics to a very simple one.

III. VEDIC MULTIPLIER

Among the 16 sutra 2 sutras are used for the multiplication. It has been found that the most efficient is Urdhva-Triyakbhyam sutra which gives min delay for multiplication of all types of numbers.

3.1. Urdhva-Tiryakbhyam - Vertically and Crosswise.

The multiplier is based on an algorithm UrdhvaTiryakbhyam (Vertical &Crosswise) of ancient Indian Vedic Mathematics. UrdhvaTiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. .
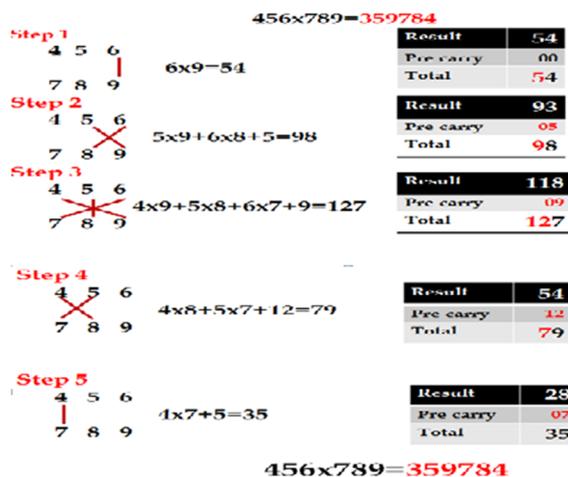Ex: Multiplication of two decimal numbers- **456x789=359784**

Fig.1 Multiplication Using Urdhva-Tiryakbhyam sutra

3.1.1. Algorithm for 4x4 Vedic multiplier

$X= A_3\ A_2\ A_1\ A_0$ Input X

$Y= B_3\ B_2\ B_1\ B_0$ Input Y

$P_0= A_0 \times B_0$

$P_1 = A_1 \times B_0 + A_0 \times B_1$

$P_2 = A_2 \times B_0 + A_1 \times B_1 + A_0 \times B_1 + C_1$

$P_3 = A_3 \times B_0 + A_2 \times B_1 + A_1 \times B_2 + A_0 \times B_3 + C_2$

P4=A3xB1+A2xB2+A1xB3+C3

P5=A3xB2+A2xB3+C4

P6=A3xB3+C5
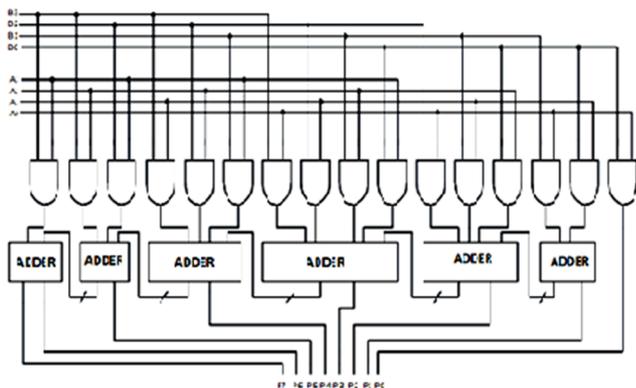
P7=C6

3.1.2.   Hard Ware Design

Fig.2. Hard Ware Design
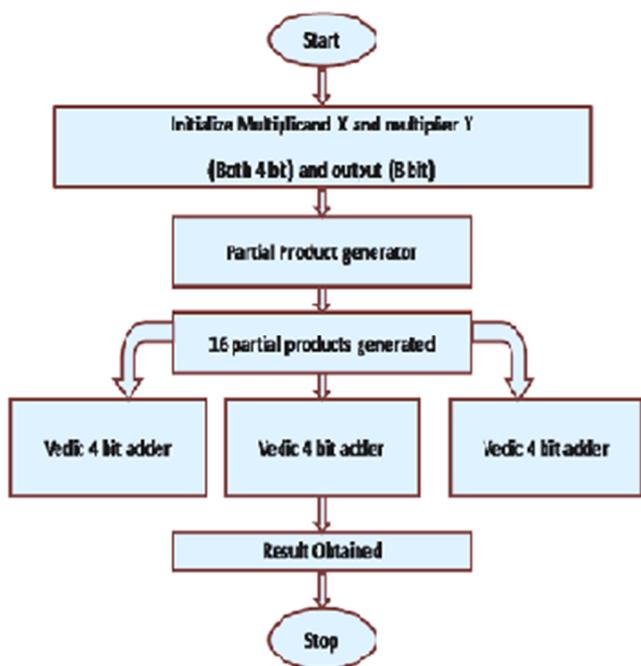
3.1.3.   Flow Chart

Fig.3. Flow Chart

IV.   ADDERS

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations. There are two basic adders, half adder and Full adder. Apart from these two adders there are four different adders

- Simple Direct Adders
- Ripple Carry Adder
- Modified Ripple Carry Adder
- Carry Look Ahead Adder

4.1   Simple Direct Adder

The Simple Direct Adder is constructed using the inbuilt functions. The 2 inputs A and B are added by the convolution method by using the simple addition method using the addition symbol "+"the equation is C=A+B.
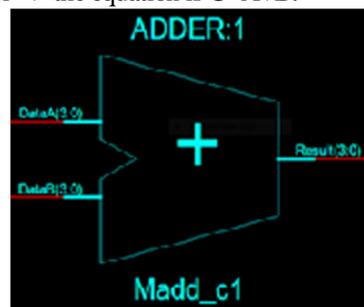

Fig.4. Simple Direct Adder Design

4.2   Ripple Carry Adder (RCA)

It is possible to create a logical circuit using multiple full adders to add *N*-bit numbers. Each full adder inputs a C_{in}, which is the C_{out} of the previous adder. This kind of adder is called a *ripple-carry adder*, since each carry bit "ripples" to the next full adder. In a 4-bit ripple-carry adder, there are 4 full adders, so as the no of bit increase there will be increase in the delay.
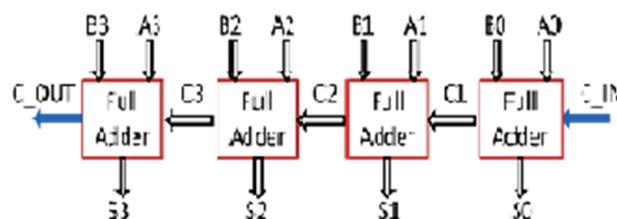

Fig.5. Ripple Carry Adder (RCA)

4.3.   Modified RCA

This adder is same as that of Ripple carry adder, instead of all full adders the starting is half adder and remaining adders are full adders. The delay decreases compared to the normal Ripple Carry adder.
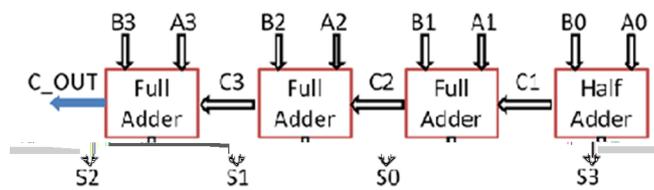

Fig.6. Modified RCA

4.4.   Carry Look Ahead Adder

A carry look ahead adder improves speed by reducing the amount of time required to determine carry bits, uses the concepts of *generating* and *propagating* carries. The carry

the sum, which reduces the wait time to calculate the result of the larger value bits.
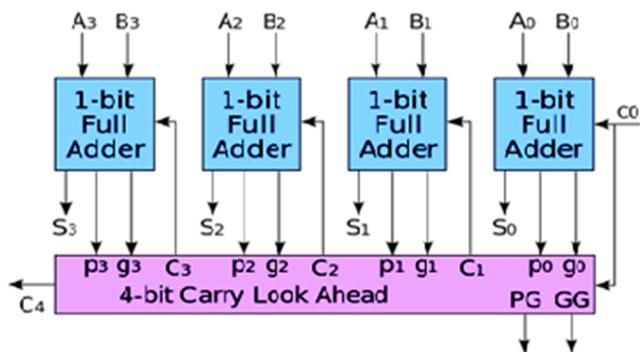

Fig.7. Carry Look Ahead Adder

V.   DESIGN

The designing of Vedic Multiplier is based on a novel technique of digital multiplication which is quite different from the conventional method of multiplication like add and shift. Here smaller blocks are used to design the bigger one. The Vedic Multiplier is designed in Verilog HDL, as it gives effective utilization of structural method of modeling.The individual block is implemented using Verilog hardware description language
.

5.1   Implementation of Vedic Multipliers Using Simple   Direct Adder (SDA)
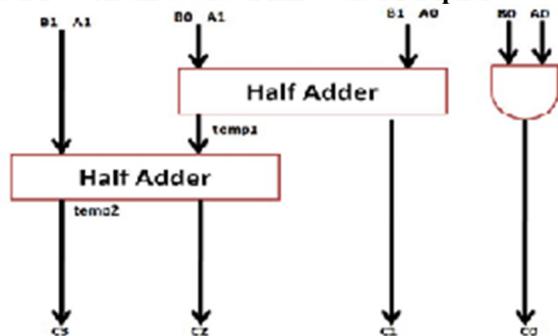
5.1.1   Architecture of 2x2 Vedic Multiplier

Fig.8. Architecture of 2x2 Vedic Multiplier

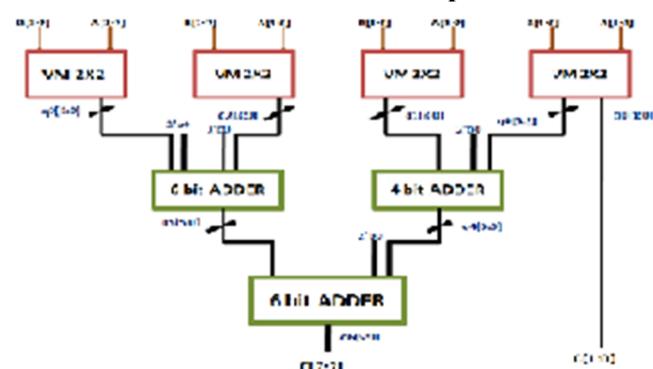#### 5.1.2   Architecture of4x4 Vedic Multiplier

Fig.9. Architecture of   4x4 Vedic Multiplier

5.1.3   Architecture of 8x8 Vedic Multiplier
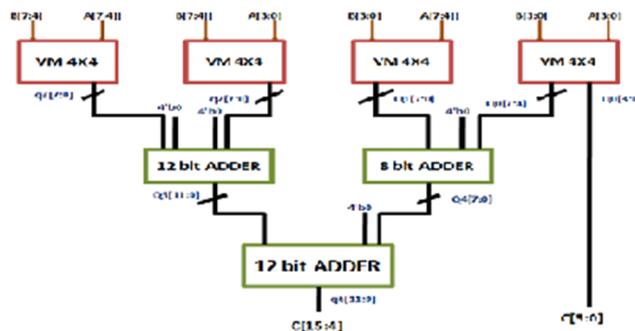

Fig.10. Architecture of 8x8 Vedic Multiplier

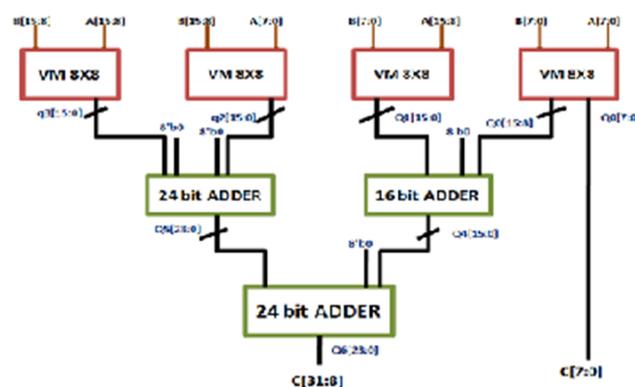#### 5.1.4   Architecture of 16x16 Vedic Multiplier

Fig.11. Architecture of 16x16 Vedic Multiplier

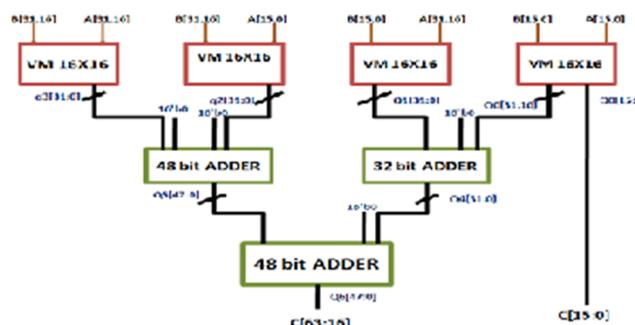#### 5.1.5   Architecture of 32x32 Vedic Multiplier

Fig.12. Architecture of 32x32 Vedic Multiplier

VI. RESULTS

6.1. 2x2 Vedic Multiplier Xilinx simulations

Fig.13. 2x2 Vedic Multiplier Xilinx simulations

6.2. 4x4 Vedic Multiplier Xilinx simulations

Fig.14. 4x4 Vedic Multiplier Xilinx simulations

6.3. 8x8 Vedic Multiplier Xilinx simulations
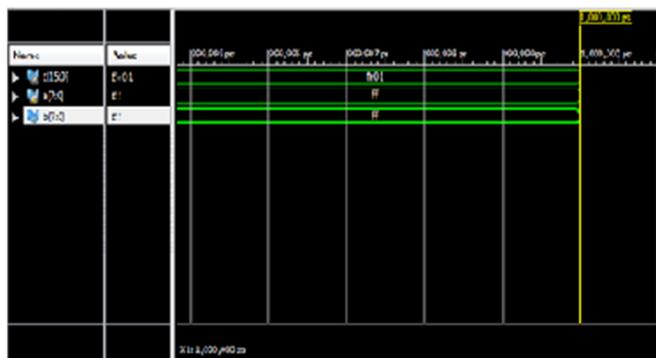
Fig.15. 8x8 Vedic Multiplier Xilinx simulations

6.4. 16x16 Vedic Multiplier Xilinx simulations

Fig.16. 16x16Vedic Multiplier Xilinx simulations

6.5. 32x32 Vedic Multiplier Xilinx simulations

Fig.17. 32x32Vedic Multiplier Xilinx simulations

6.6. Comparison Table using Xilinx

VM Adder	Simple Adder	CLA	RCA	Modified RCA
Vedic 2x2	5.735ns	5.735ns	5.735ns	5.735ns
Vedic 4x4	12.007ns	13.209ns	13.201ns	13.201ns
Vedic 8x8	15.112ns	19.284ns	18.134ns	18.472ns
Vedic 16 x16	19.254ns	30.315ns	32.015ns	28.609ns
Vedic 32x32	23.848ns	52.316ns	53.941ns	45.682ns

Table.1. Delay Comparison Table using Xilinx

6.7. Delay Comparison Table using Cadence

VM Adder	Simple Adder(Ps)	CLA(Ps)	RCA(Ps)	Modified RCA (Ps)
Vedic 2x2	165	165	165	165
Vedic 4x4	844	1024	1068	1031
Vedic 8x8	1664	2086	2406	2255
Vedic 16 x16	2723	3832	4794	4453
Vedic 32x32	4055	6956	9282	8600

Table.2. Delay Comparison Table using Cadence

6.8. Area Comparison Table using Cadence

VM Adder	Simple Adder	CLA	RCA	Modified RCA
Vedic 2x2	48	48	48	48
Vedic 4x4	751	559	703	613
Vedic 8x8	4529	2961	3826	3376
Vedic 16 x16	21987	13238	17329	15437
Vedic 32x32	97409	56058	73356	65698

Table.3. Area Comparison Table using Cadence

6.9. Power Comparison Table using Cadence

VM Adder	Simple Adder(nw)	CLA(nw)	RCA(nw)	Modified RCA(nw)
Vedic 2x2	843.465	843.465	843.465	843.465
Vedic 4x4	9884.009	10425.695	11420.271	10362.989
Vedic 8x8	67947.277	69132.563	76306.984	69825.157
Vedic 16 x16	422677.916	397183.853	441906.667	411416.607
Vedic 32x32	2370447.452	2036407.139	2294392.216	2161200.756

Table.4. Power Comparison Table using Cadence

VII. Conclusion

Urdhva tiryakbhyam, being general mathematical formula, is equally applicable to all cases of multiplication. A multiplier architecture based on this Sutra has been developed and used different types of adders for comparative study in detail. Here simple direct adder has less delay compared to other adders.

VIII. Future Scope

Vedic mathematics deals with various topics of mathematics such as basic arithmetic, geometry, trigonometry, calculus etc. All these methods are very efficient as far as manual calculations are concerned. If all those methods effectively implement hardware, it will reduce the computational speed drastically. Therefore, it could be possible to implement a complete ALU using all these methods using Vedic mathematics methods. Vedic mathematics is long been known but has not been implemented in the DSP and ADSP processors employing large number of multiplications in calculating the various transforms like FFTs and the IFFTs. By using these ancient Indian Vedic mathematics methods world can achieve new heights of performance and quality for the cutting edge technology devices.

IX.   References

[1] FPGA Implementation of a 4×4 Vedic Multiplier by S.Panigrahi, O P Das, B B Tripathy, T K Dey InternationalJournal of Engineering Research and Development e-ISSN 2278-067X, p-ISSN: 2278-800X

[2] HIGH SPEED VEDIC MULTIPLIER DESIGNS by Yogita Bansal, Charu Madhu ,Pardeep Kaur978-1-4799-2291-8/14/$31.00 ©2014 IEEE

[3] Propagation delay based comparison of parallel adderby HEMOZHI.G, THENMOZHI.V Journal of Theoretical and Applied Information Technology ISSN: 1 92-8645 ,
 E-ISSN: 1817- 3195

[4] Design of Low Power and High Speed Modified Carry Select Adder for 16 bit Vedic Multiplier by Bhavani Prasad.Y, Ganesh Chokkakula, Srikanth Reddy.P and Samhitha.N.RISBNNo.978-1-4799-3834-6/14/$31.00©2014 IEEE

[5] Comparison of a 32-Bit Vedic Multiplier With A Conventional Binary Multiplier Abhyarthana Bisoyil, Mitu Baratl, Manoja Kumar Senapati ISBN No. 978-1-4799-3914-5/14/$31.00 ©2014 IEEE