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FIVE-LEVEL INVERTER SWITCHING FOR THE OPEN-END WINDING IM DRIVE TO ACHIEVE COMMON MODE VOLTAGE ELIMINATION AND DC-LINK CAPACITOR VOLTAGE BALANCING

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Abstract

A variation of Common mode voltage (CMV) in PWM inverter-fed drives causes unbalanced voltage operation in induction motor. Multilevel inverters reduce this problem to some extent, but the complexity of the power circuit increases with an increase in the number of inverter voltage levels. In this project a five-level inverter structure is proposed for open-end winding induction motor (IM) drives. It consists of cascaded two conventional two-level and three-level inverters, this inverter scheme do not experience neutral-point fluctuations.

This project work carried for generation of five level inverter output voltage open-end winding induction motor drive. Multilevel carrier-based SPWM used for generating the gate pulses of the cascaded inverters of the proposed drive. The proposed work carried by using MATLAB.

Keywords: *Inverter, Inverter Structure, IM Drive*

I. Introduction

The complexity of the power circuit increases as the number of voltage levels increases in the multi-level inverters. As a consequence, the neutral point clamped (NPC) inverter with more than three levels is seldom utilized for motor drives. The conventional NPC three-level inverter is characterized with the problem of neutral point voltage fluctuation and this voltage fluctuation causes unbalance in the DC-link capacitor voltages. Unbalance in capacitor voltages leads to excessive voltage stress on the switching devices and generates low order harmonic currents, resulting in torque pulsation.

As the number of levels increases, the number of DC-link capacitors will increase and balancing of the capacitor voltages becomes very difficult. Due to the low number of Redundant switching states in the voltage space vector locations, DC-link capacitor voltage balancing is very difficult in the conventional NPC inverters, especially in the high modulation range. Available DC-link capacitor voltage balancing schemes tend to use additional circuits, such as buck-boost converter or controlled front-end converters. [1]

If a motor drive is with an open-end stator winding structure rather than with a star-connected stator winding, multi-level inverter supply schemes can be realized by supplying the two sides of the windings with inverters of a certain number of levels. Combined CMV elimination and capacitor Voltage balancing scheme for a five-level inverter-fed open-end winding IM drive has been proposed.

In this paper, combined CMV elimination and capacitor voltage balancing are discussed in conjunction with an open-end winding induction motor drive. Compared to the power circuit structure employed in, the configuration utilized in this paper is considerably simpler. The scheme described here is capable of maintaining the DC-link capacitor voltages for both motoring and generating mode of operation, without affecting the output fundamental.

Due to the power circuit five-level inverter structure of, some of the switching states are not available, resulting in a lower number of redundant switching states. But the available for the voltage space vector locations of the proposed five level inverter are sufficient to maintain the balance in DC-link Capacitor voltages for the entire speed of operation with the elimination of the common mode voltage. No extra is required for the DC-link capacitor voltage balancing.

3. Elimination of the Common Mode Voltage

Power circuit configuration of the five-level inverter structure for an open-end winding induction motor drive, Analyzed in this paper, is shown in Fig. 4.1.

To start with, there is a single DC-link voltage. There are a total of two two-level and two three-level inverters. Each of the two inverter systems (A and A') consists of a series-connected NPC three-level inverter and the conventional two two-level inverters. The two-level inverters are shared by both inverter systems A and A', as shown in Fig. 4.1.

Each two-level/three level inverter combination will produce a five-level voltage space vector structure. The combined multi-level inverter will therefore produce a nine-level voltage space vector structure. However, not all of the available voltage space vectors are characterized with switching states leading to the zero CMV. Hence only those switching states that yield zero CMV are selected for the PWM operation in this study, resulting in a combined five-level voltage space vector structure.

3.1 DC-Link Capacitor Voltage Control – An Open loop Method

In the open-loop method the power circuit of Fig.-4.1 with a single DC-link is analyzed for DC-link capacitor voltage balancing of all the four capacitors. Let the currents through the middle points of the capacitors C_4, C_3; C_3, C_2; and C_2, C_1 are denoted as i_3 , i_2 and i_1 , respectively. Then the following holds true:

$$V_{C4} - V_{C3} = \frac{1}{C}\int i_3\, dt$$

$$V_{C3} - V_{C2} = \frac{1}{C}\int i_2\, dt$$

$$V_{C2} - V_{C1} = \frac{1}{C}\int i_1\, dt$$

From the above equations, it follows that the DC-link capacitor voltages vc_4, vc_3, vc_2 and vc_1 will be equal if the currents i_3, i_2 and i_1 are Zero. Hence, to maintain the balance in the DC-link capacitor voltages, it is necessary to make all these three currents equal to zero. The aim of the selection of the switching states for the voltage vectors is here to simultaneously eliminate the common mode voltage and to eliminate the DC-link capacitor voltage unbalancing.

For the elimination of the CMV, only those switching states that have the zero CMV are switched for the PWM operation, as already explained in the preceding section (Table I). The same switching states from a particular location, having opposite effect on the capacitor voltages, are used in the present study for open-loop voltage control. Selection of the switching states for open-loop control of capacitor voltages is explained in the following two sections.[2]

3.2 Closed-Loop Control of Dc-Link Capacitor Voltage Balancing

A simple hysteresis controller is used for the closed-loop control of the DC-link capacitor voltage balancing. A Hall effect sensor is used to sense the voltages across the DC-link capacitors. The input to the controller will be the difference of the two capacitor voltages (the controller has two inputs, the difference between the outer two capacitor voltages and the difference between the inner two capacitor voltages). The controller will sense the unbalance in the capacitor voltages from the voltage difference. The controller will take the corrective action only if the difference of the voltages between the two capacitors exceeds the specified hysteresis band. The Error band can be specified for the hysteresis controller depending on the voltage rating of the devices and the Maximum error allowable for the system.

Fig.1 shows the proposed hysteresis controller block diagram for the closed loop control scheme of the DC-link capacitor voltage balancing. There are two comparators, as shown in Fig.-6.1, that continuously compare the difference between the outer two and the inner two DC-link capacitor voltages. The outputs of the comparators are fed to the hysteresis controller. There will be three different states for each group (C_1 and C_4 are in group-1, C_2 and C_3 are in group-2) of the DC-link capacitor voltages and these are identified as C_H, C_N, C_L.

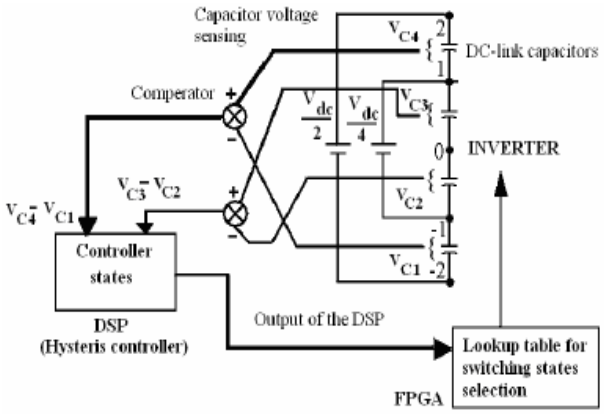

Fig.-1 : Hysteresis controller for the closed-loop control of the dc-link capacitor voltage balancing

Table 6.1 shows the states for various DC-link capacitor voltage differences, for each group of capacitors. These states are called the controller states, as the controller will select those inverter switching states for balancing the voltages across the DC-link capacitors.

TABLE – 1 : Controller states for the different dc-link capacitor voltage conditions (Capacitors C_4, C_1 and C_3, C_2).

Capacitor Voltage difference	States
$V_{C4} - V_{C1} > 0$	C_{1H}
$V_{C3} - V_{C2} > 0$	C_{2H}
$V_{C4} - V_{C1} = 0$	C_{1N}
$V_{C3} - V_{C2} = 0$	C_{2N}
$V_{C4} - V_{C1} < 0$	C_{1L}
$V_{C3} - V_{C2} < 0$	C_{2L}

The combinations from the two comparator outputs of Fig.6.1 will generate nine controller output states, identified as follows:

$C_{1H}\ C_{2H}$, $C_{1H}\ C_{2N}$, $C_{1L}\ C_{2N}$

$C_{1N}\ C_{2N}$, $C_{1N}\ C_{2H}$, $C_{1N}\ C_{2L}$

$C_{1H}\ C_{2L}$, $C_{1L}\ C_{2H}$, $C_{1L}\ C_{2L}$

4. Simulation Results

To check the controller Action at every level of operation, the closed-loop controller is disabled for a moment and then again enabled. It can be observed that the deviation due to disabling of the controller is brought back to the normal state quickly once the controller is enabled.

In two-level and three-level operation (Fig.-4.1 and Fig.-4.2), it can be noted that there is no effect on *vc*1 and *vc*4 due to disabling of the controller, while voltages *vc*2 and *vc*3 are affected. But from four-level to 12-step mode of operation, deviation occurs in all the four capacitor voltages due to the disabling of the controller. [3] [4]

4.1 TWO LEVEL INVERTER :

For the two level inverter, the phase voltage and phase current are shown in fig.-4.1(a).

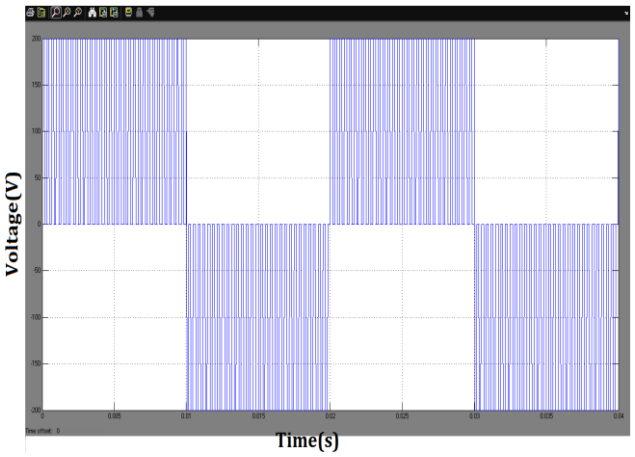

Fig.- 4.1 (a) : phase voltage for the two-level operation

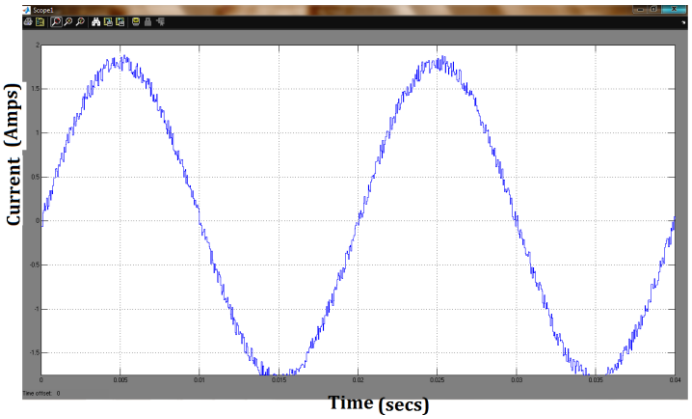

Fig.- 4.1 (a) : phase current for the two-level operation

The variation of capacitor voltages during disabling and enabling of control is shown in fig.-4.1(b).

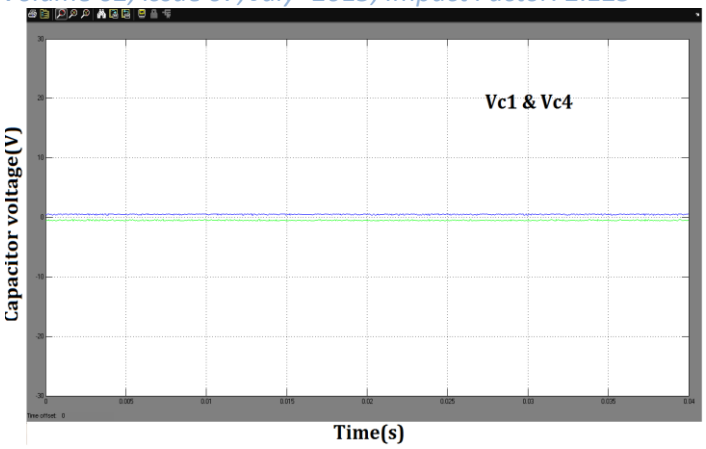

Fig.- 4.1(b) : variation of capacitor voltages during disabling and enabling of control

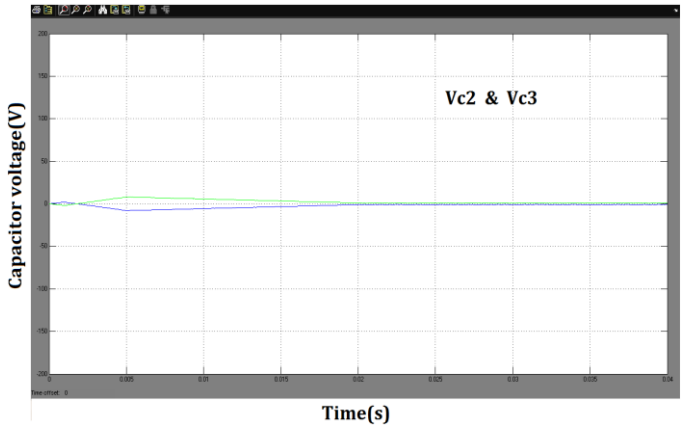

Fig.- 4.1(b) : variation of capacitor voltages during disabling and enabling of control

The system is brought back quickly to the normal state, once the controller is enabled. As the PWM controller moves to the higher levels of operation (five level, over-modulation and 12-step operation), it can be noted that restoring of the capacitor voltages back to the normal state takes more time, when compared to the operation in the inner layers. This is due to the fact that the number of available redundant switching states reduces, as the speed (voltage) increases.

4.2 <u>THREE LEVEL INVERTER</u> :

For the three level inverter, the phase voltage and phase current are shown in fig.-4.2(a).

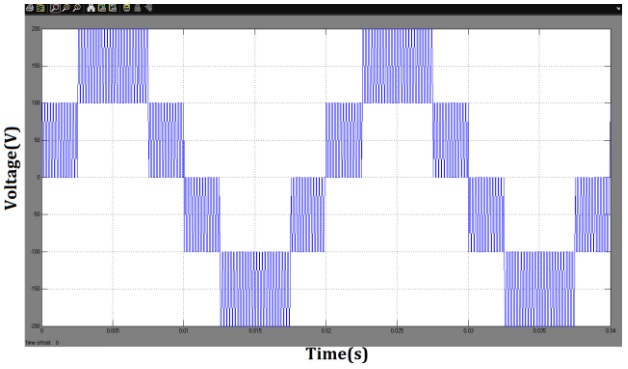

Fig.- 4.2 (a) : phase voltage for the three-level operation

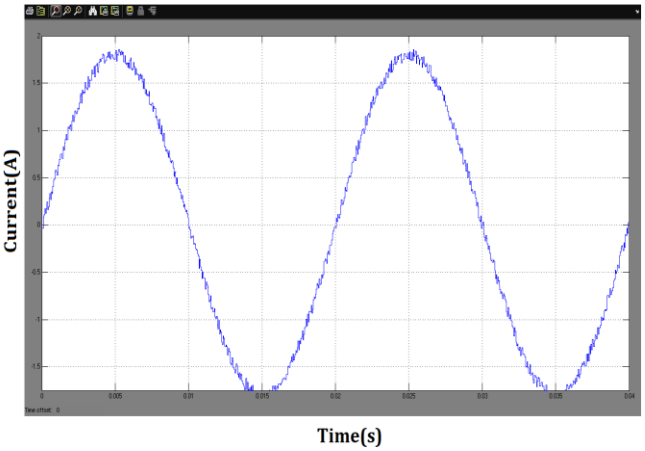

Fig.- 4.2 (a) : phase current for the three-level operation

The variation of capacitor voltages during disabling and enabling of control is shown in fig.-4.2(b).

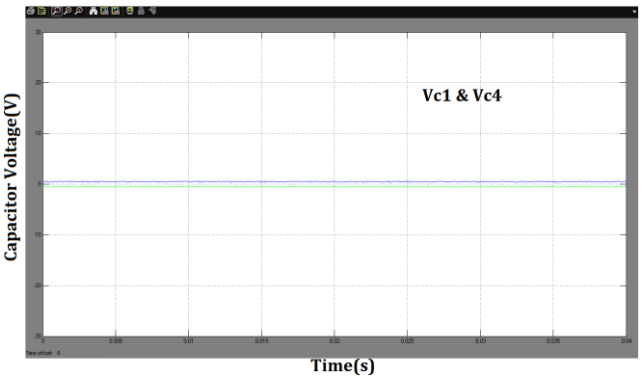

Fig.- 4.2(b) : variation of capacitor voltages during disabling and enabling of control

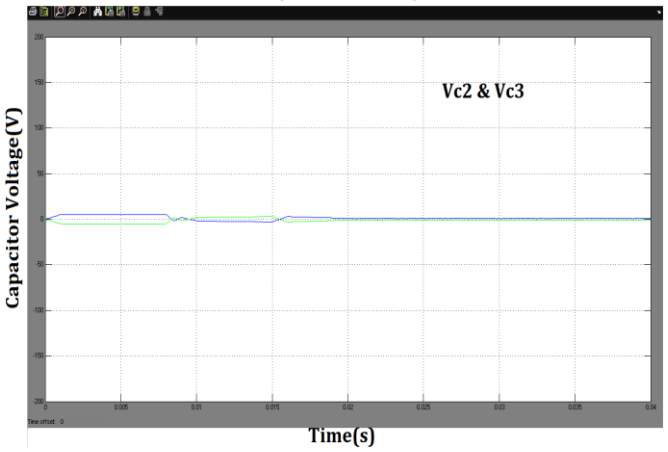

Fig.- 4.2(b) : variation of capacitor voltages during disabling and enabling of control

4.3 FOUR LEVEL INVERTER :

For the four level inverter, the phase voltage and phase current are shown in fig.-4.3(a).

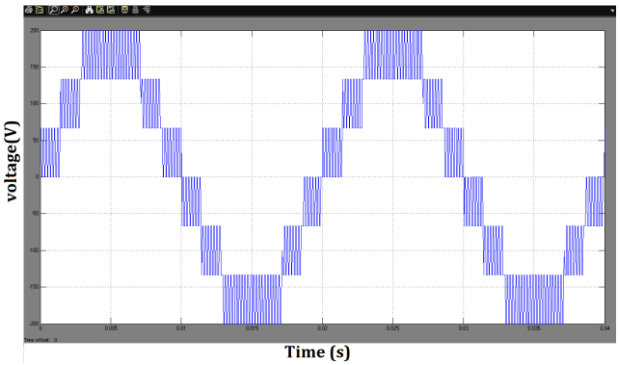

Fig.- 4.3 (a) : phase voltage for the four-level operation

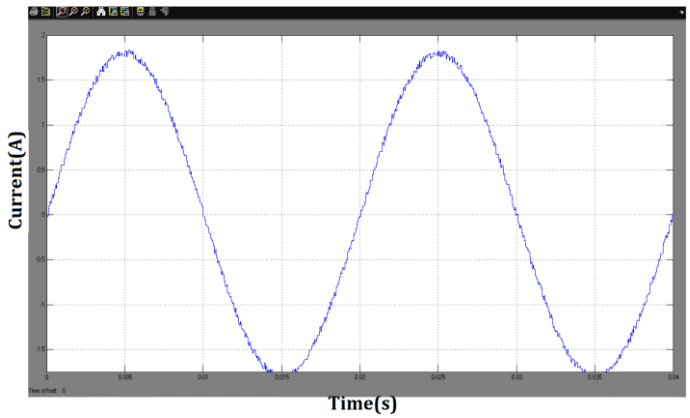

Fig.- 4.3 (a) : phase current for the four-level operation

The variation of capacitor voltages during disabling and enabling of control is shown in fig.-4.3(b).

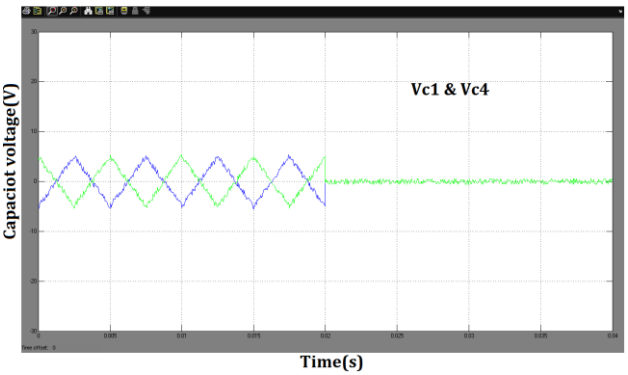

Fig.- 4.3(b) : variation of capacitor voltages during disabling and enabling of control

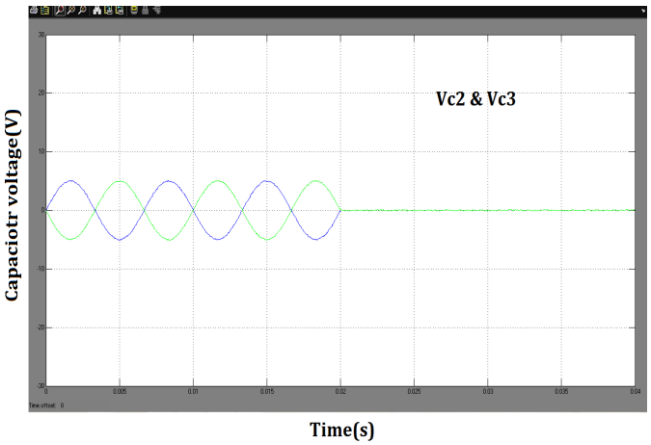

Fig.- 4.3(b) : variation of capacitor voltages during disabling and enabling of control

4.4 FIVE LEVEL INVERTER :

For the five levels inverter the phase voltage and phase current are shown in fig.-4.4(a).

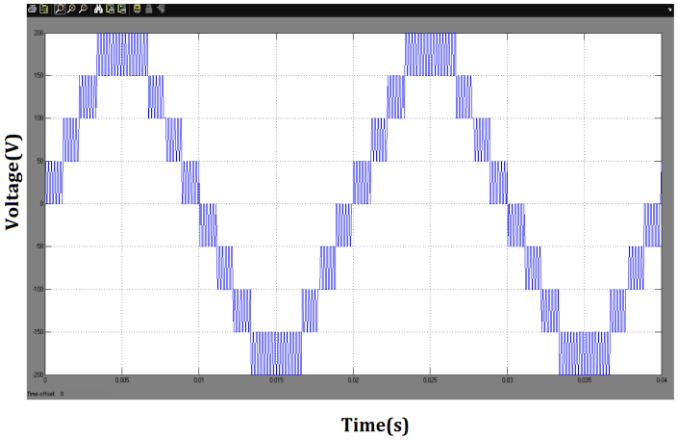

Fig.- 4.4 (a) : phase voltage for the five-level operation

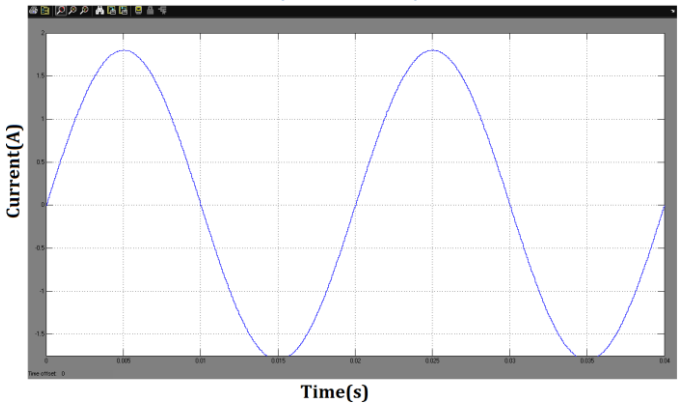

Fig.- 4.4 (a) : phase current for the five-level operation

The variation of capacitor voltages during disabling and enabling of control is shown in fig.-4.4(b).

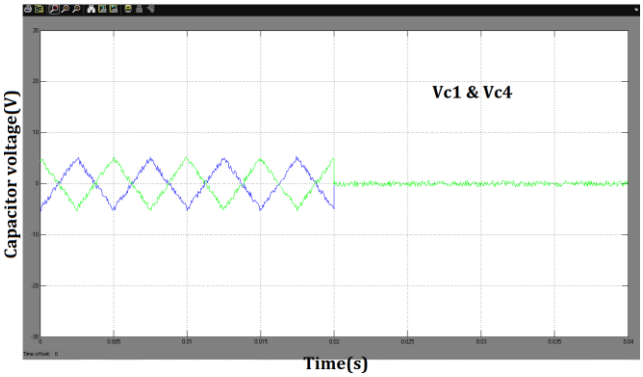

Fig.- 4.4(b) : variation of capacitor voltages during disabling and enabling of control

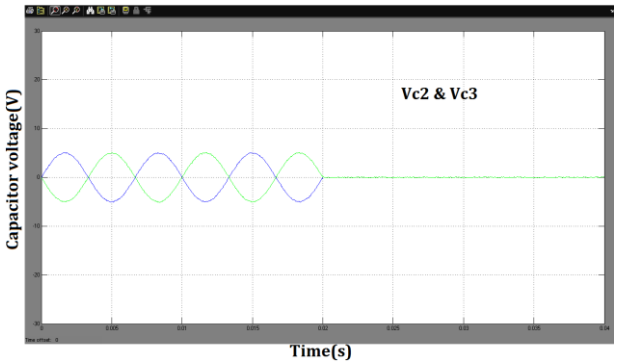

Fig.- 4.4(b) : variation of capacitor voltages during disabling and enabling of control

For the over-modulation region the phase voltage and phase current are shown in fig.-4.5(a).

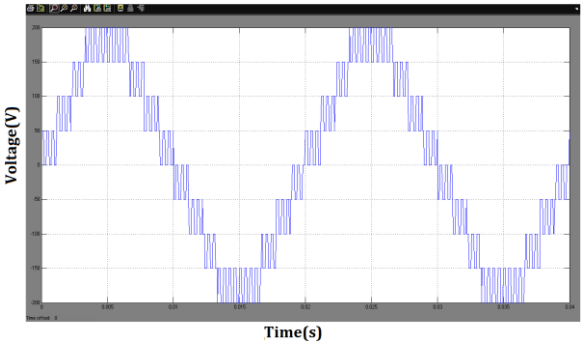

Fig.- 4.5 (a) : phase voltage in over-modulation region

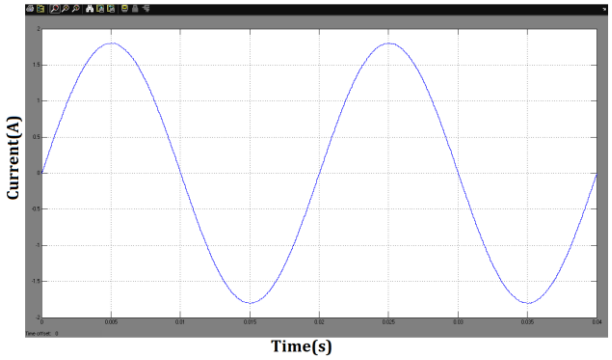

Fig.- 4.5 (a) : phase current in over-modulation region

In over-modulation region, the variation of capacitor voltages during disabling and enabling of control is shown in fig.-4.5(b).

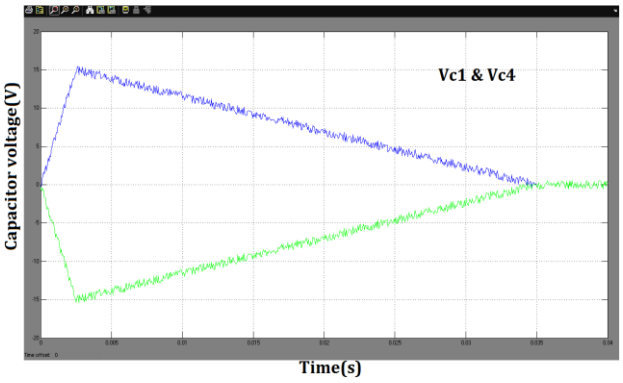

Fig.- 4.5(b) : variation of capacitor voltages during disabling and enabling of control

4.5 <u>OVER MODULATION REGION</u> :

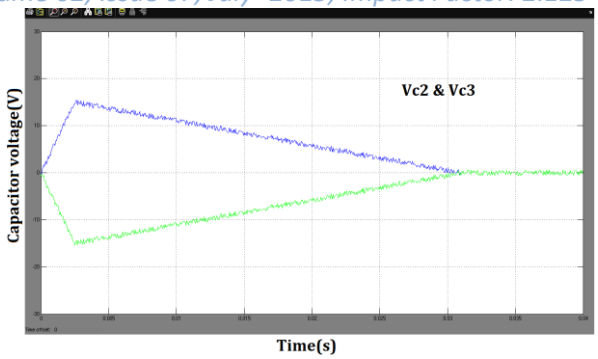

Fig.- 4.5(b) : variation of capacitor voltages during disabling and enabling of control

5. Applications

(a) DC power source utilization:

Inverter designed to provide 115 VAC from the 12 VDC source provided in an automobile. The unit shown provides up to 1.2 amperes of alternating current, or enough to power two sixty watt light bulbs.

(b) Uninterruptible power supplies :

An uninterruptible power supply (UPS) uses batteries and an inverter to supply AC power when main power is not available. When main power is restored, a rectifier is used to supply DC power to recharge the batteries.

(c) Induction heating :

Inverters convert low frequency main AC power to a higher frequency for use in induction heating. To do this, AC power is first rectified to provide DC power. The inverter then changes the DC power to high frequency AC power.

(d) HVDC power transmission :

With HVDC power transmission, AC power is rectified and high voltage DC power is transmitted to another location. At the receiving location, an inverter in a static inverter plant converts the power back to AC.

(e) Variable-frequency drives :

A variable-frequency drive controls the operating speed of an AC motor by controlling the frequency and voltage of the power supplied to the motor. An inverter provides the controlled power. In most cases, the variable-frequency drive includes a rectifier so that DC power for the inverter can be provided from main AC power. Since an inverter is the key component, variable-frequency drives are sometimes called inverter drives or just inverters.

(f) Electric vehicle drives :

Adjustable speed motor control inverters are currently used to power the traction motors in some electric and diesel-electric rail vehicles as well as some battery electric vehicles and hybrid electric highway vehicles such as the Toyota Prius. Various improvements in inverter technology are being developed specifically for electric vehicle applications.[2] In vehicles with regenerative braking, the inverter also takes power from the motor (now acting as a generator) and stores it in the batteries.

6. Conclusion

A five-level inverter for the open-end winding IM drive is developed in such a manner that both common mode voltage elimination and DC-link capacitor voltage balancing are achieved, across the entire modulation range, using only the switching state redundancies. An open–end winding configuration is used for the motor and the motor is fed from

both ends with multiple inverter structure, realized by cascading a three-level inverter with two two-level inverters. In the considered configuration the two two-level inverters are shared by the two three-level inverters at both ends of the motor stator winding. This will make the power circuit simpler to fabricate, when compared to any of the other existing topologies.

A simple closed-loop control scheme, based only on the switching state redundancy, is suggested for the closed loop control of the DC-link capacitor voltage balancing. The present scheme has the capability of maintaining the DC-link capacitor voltage balance, and also has the ability to take the quick corrective action, if any unbalance occurs in the capacitor voltages. The available redundant switching states are effectively used for the common-mode voltage elimination and capacitor voltage balancing without adding extra hardware for achieving the capacitor voltage balancing, and without affecting the fundamental output voltage of the inverter.

Experimental results from 2.5 KW drive are presented and these confirm the capability of the developed scheme to Provide the balancing of the DC-link capacitor voltages and CMV elimination for the entire range of operation, using only the switching state redundancies. The presented multi-level inverter-fed scheme can be extended to other structures with a higher overall number of levels by further cascading the conventional inverter structures.

7. References

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