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DESIGN AND ANALYSIS OF FIVE LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER USING LEVEL SHIFTED PWM

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Abstract—*This Dissertation is dedicated to performance analysis of five level cascaded multilevel inverter using level shifted pwm. Nowadays, the industries required additional power with low harmonics for the high power applications. Multilevel Inverters becoming trendier for the high power applications due to fewer amounts of harmonics and high power ratings so this concept is introduced. The importance of the multilevel converters has been increase since the last decade. The ability to synthesize waveforms for high voltage with better harmonic spectrum, these new types of multilevel converters are suitable for high power applications. Thus Multilevel Inverter concept is introduced. Several topologies have been described, amongst these topologies, the Cascaded H-bridge Multilevel Inverter is proposed due to its having several advantages over other two topologies. Also the modulation topologies (PWM techniques) for multilevel inverters are proposed. The proposed topologies are IPD (In-phase Disposition), POD (Phase Opposition Disposition) and APOD (Alternate Phase Opposition Disposition). These modulation strategies reduce the Total Harmonic Distortion and it enhances the fundamental output voltages. The simulations for the IPD, POD and APOD are carried out for Single phase and three phase Open loop and closed loop configurations in MATLAB/Simulink software. Also %THD results are taken and analyzed for the single phase and three phase multilevel inverter for open loop configuration. The comparative results analysis for %THD is given for Single phase and three phase Open loop and closed loop configuration.*

Key Words*: Cascade H-bridge multilevel inverter, SPWM, THD, IPD, POD, APOD*

I. INTRODUCTION

Nowadays industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV). Many industrial applications have begun to require higher power apparatus in recent years [1]. Some medium voltage motor drives and power utility applications require medium voltage and megawatt power level. In the medium voltage power utility system, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages [1]. The term multilevel starts with the three-level inverter introduced by Nabae et al. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. The results of a patent search show that multilevel inverter circuits have been around for more than 25 years [1]. The multilevel inverter using cascaded inverter with Separate DC Source synthesizes a desired voltage [8] Output voltages of three-level inverter are built from three state voltage combination, so the voltage wave is more like sinusoidal form than two-level inverter. Hence, the output current ripple is lower at the same switching frequency [4].The main function of the multilevel inverter is to synthesize a desired voltage wave from several levels of dc voltages. Due to this reason, multilevel inverters provide the high power required of a large electric drive. Also, due to more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels increases. As the number of level increases, the voltage that can be extended by summing multiple voltage levels. Due to the structural property of the multilevel inverter no voltage sharing problems are encountered by the active devices. It exhibits several attractive features such as simple circuit layout, less components counts, modular in structure and avoid unbalance capacitor voltage problem. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. So the multilevel inverter from several independent sources of dc voltages, which may be obtained from batteries, fuel cells or solar cells [2].

A. Concept of Multilevel Inverter

Basically Inverter is a device that converts DC power to AC power at desired output voltage and frequency. Demerits of inverter are less efficiency, high cost, and high switching losses. To overcome these demerits, we are going to multilevel inverter. The multilevel inverter output voltage having less number of harmonics compare to the conventional bipolar inverter output voltage. If the multilevel inverter output increase to N level, the harmonics reduced to the output voltage value to zero [1]. Multilevel system is popular because of it advantages, the inverter can produce medium or high AC voltage by using low switching frequency. By using low switching frequency, switching losses is decreased so that the inverters efficiency is increased.

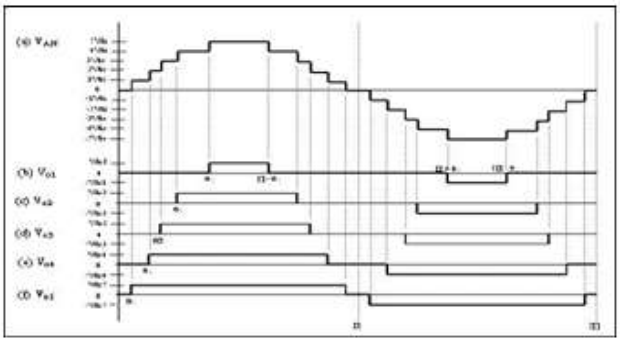

Fig.1 Multilevel inverter levels [24]

There are several types of multilevel inverter as discussed below:
I. Diode-clamped multilevel inverter
II. Flying capacitor multilevel inverter
III. Cascaded H-bridge multilevel inverter

B. Cascaded H-bridge Multilevel Inverter

One more topology for a multilevel inverter classified in previous is the cascaded multilevel inverter or Cascaded H-bridge multilevel inverter. Cascaded multilevel inverter was not completely realized without two researchers, Lai and Peng. In 1996, Lai and Peng patented and presented the basic model of CHB multilevel inverter [1]. The Cascaded H-bridge inverter synthesizes its output voltage closely to the sinusoidal voltage waveforms by adding many different voltage levels.

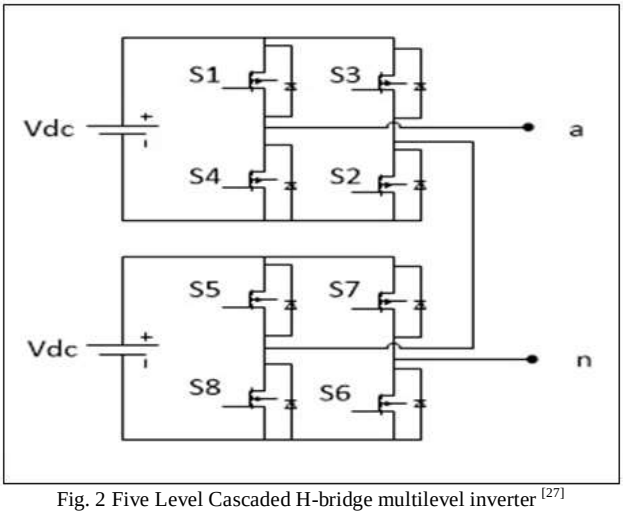

Fig. 2 Five Level Cascaded H-bridge multilevel inverter [27]

Fig. 2 shows the power circuit of a five level inverter with two cells in each phase. The resulting phase voltage is obtained by the addition of the voltages generated by the different cells. Each single phase bridge inverter generates three voltages at the load side or output: +Vdc, 0 and –Vdc. This is only achievable by connecting the dc source in order to ac side via the four switches. The resultant output ac voltages swings from -2Vdc to 2Vdc with five levels, and the staircase waveform is obtained with nearly to the sinusoidal waveform even without filtering.

II. MODULATION TOPOLOGIES FOR MLI

The multilevel inverter is used for high frequency and power applications so among all the techniques Sinusoidal PWM technique is described. There are basically two types of SPWM one is Phase Shifted PWM and another is Level Shifted PWM.

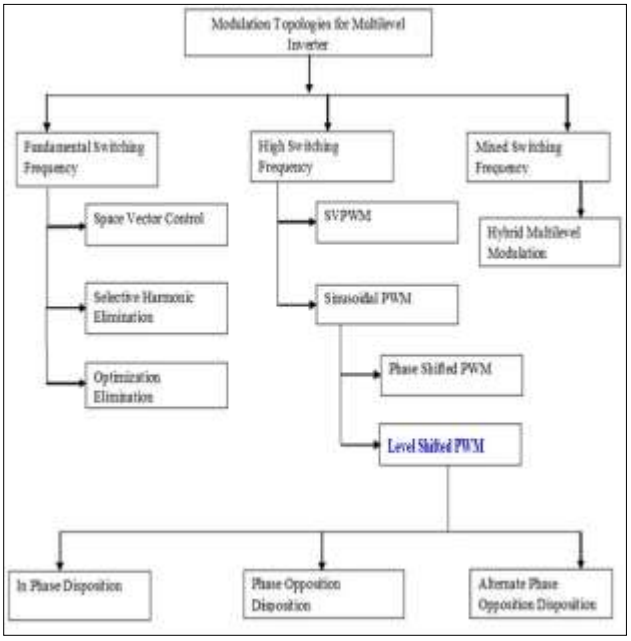

Fig. 3 Classification of Multilevel inverter modulation topologies

III. BLOCK DIAGRAM OF PROPOSED TOPOLOGY

The below figure shows the basic block diagram of proposed topology.

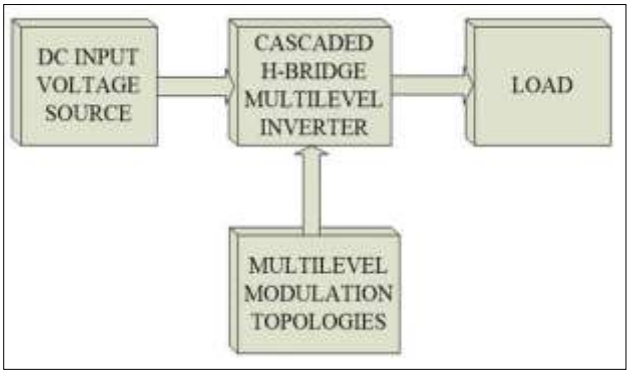

Fig. 4 Basic block diagram of proposed topology

A. PI CONTROLLER

The block diagram of PI controller is shown below.

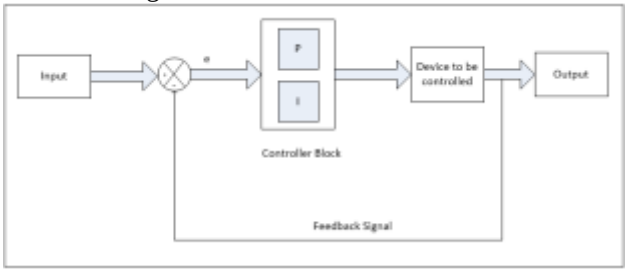

Fig. 5 PI Controller block diagram

In the PI controller, the term integral improves by reducing the error signal which is generated by the reference and the actual voltage. The error is required to maintain the range which is defined by the triangular wave amplitude. As a result, the error signal

is compared with a triangular signal and the pulse which are generated by intersections of the error signal and triangular signal which decide the switching frequency and pulse width. PI controller is also known as feedback controller in which the difference between output signal and desired or reference signal generates the error value. PI controller is used to eliminate this error by controlling the system inputs P and I. Proportional part (P) minimize the error while Integral part (I) minimizes the offset which can balance the whole system. P depends on present error and I depend on past errors. So, by using PI controller the step response of a system can be improved.

B. PHASE LOCKED LOOP (PLL)

The PLL is used to provide a unity power factor operation, which involves synchronization of the inverter output current with the grid voltage and to give a clean sinusoidal current reference. LPF is used to extract the low harmonic frequency component in the supply. There are several PLL algorithms with different characteristics. However, despite of their differences, all PLL algorithms have three main sections: Phase detector (PD), Filter and Voltage Controlled Oscillator (VCO). The PI controller parameters of the PLL structure are calculated in such a way that we can set directly the settling time and the damping factor of this PLL structure. The generated error angle in degree is then added to the reference angle (which is generated using carrier source having ramp of 0 to 360 and frequency of 50 Hz). The PLL structure is used for grid voltage monitoring in order to get the phase and the frequency values of the grid voltage. The basic block diagram of PLL is as shown in below fig. 6.

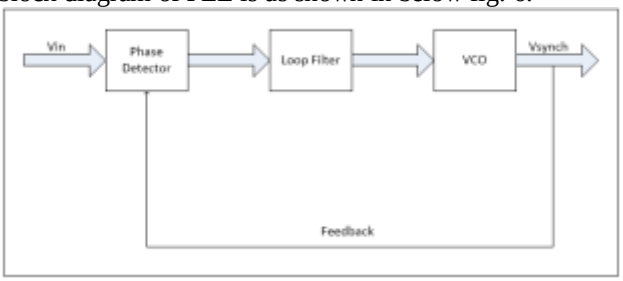

Fig. 6 Block diagram of PLL

IV. SIMULATIONS AND RESULTS

Simulink model and results of Single phase Open loop Five level inverter for In Phase Disposition (IPD):

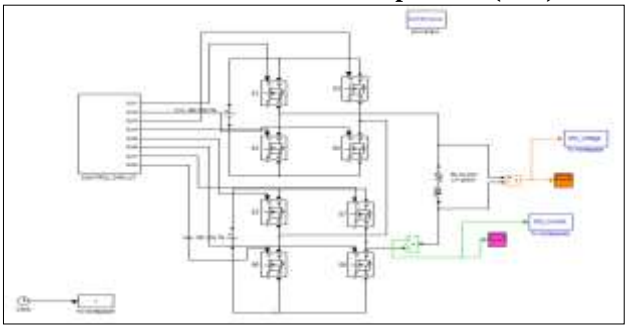

Figure 7.Simulink model of Single phase Open Loop In Phase Disposition

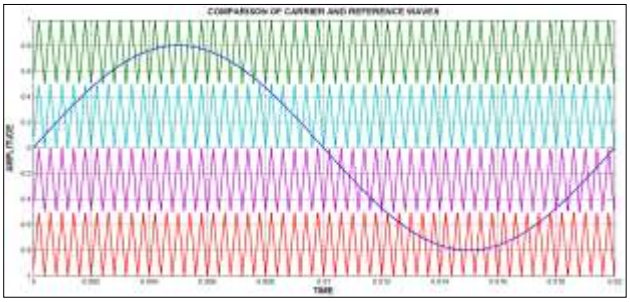

Fig. 8 Comparison of Reference and Carrier Waves for In phase Disposition

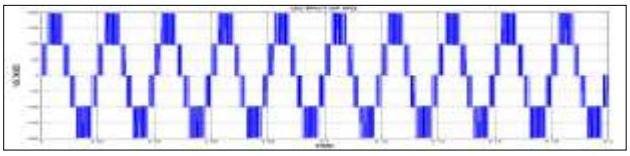

Fig. 9 Output voltages for In phase Disposition

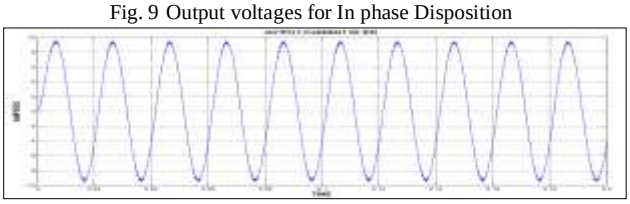

Fig. 10 Output current for In phase Disposition

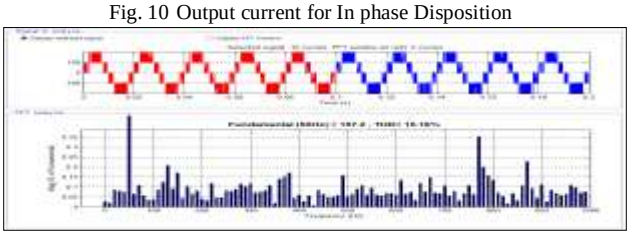

Fig. 11 %THD of Voltage for In phase Disposition (%THD= 15.18%)

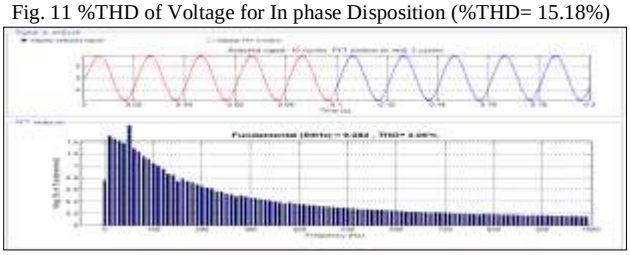

Fig. 12 %THD of Current for In phase Disposition (%THD= 2.00%)

Table 1.%THD analysis of Single phase Open loop Five level CHB Inverter

	Modu. Index	Fund. Voltage	Voltage THD (%)	Current THD (%)
SINGLE PHASE OPEN LOOP IPD	0.6	118	21.38	2.03
	0.7	137.7	18.48	2.04
	0.8	**157.2**	**15.18**	**2.00**
	0.9	176.7	14.98	2.00
	1.0	196.2	12.07	1.98
SINGLE	0.6	118	20.98	2.04
	0.7	137.7	18.43	2.03

PHASE OPEN LOOP POD	**0.8**	**157.2**	**15.39**	**2.00**
	0.9	176.8	15.12	1.99
	1.0	196.2	12.15	1.97
SINGLE PHASE OPEN LOOP APOD	0.6	117.9	20.98	2.03
	0.7	137.6	19.10	2.01
	0.8	**157.2**	**14.94**	**2.01**
	0.9	176.6	14.86	1.99
	1.0	196.2	12.16	1.98

Simulink model and results of Three Phase Open Loop Five Level Inverter for Phase Opposition Disposition:

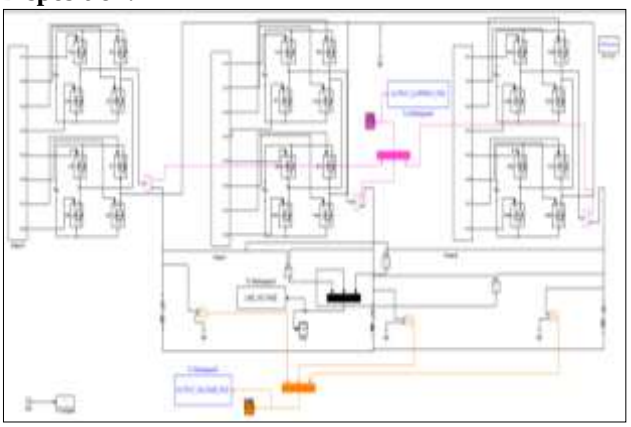

Fig. 13 Simulink model of Three phase Open Loop Phase Opposition Disposition

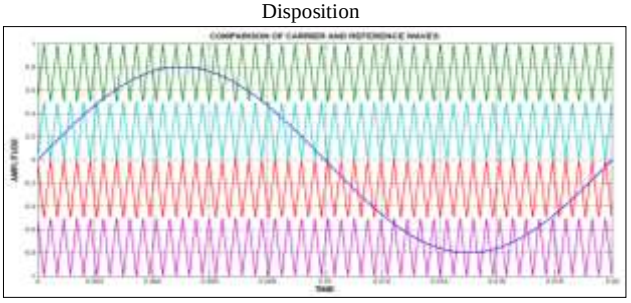

Fig. 14 Comparison of carrier and reference wave for POD

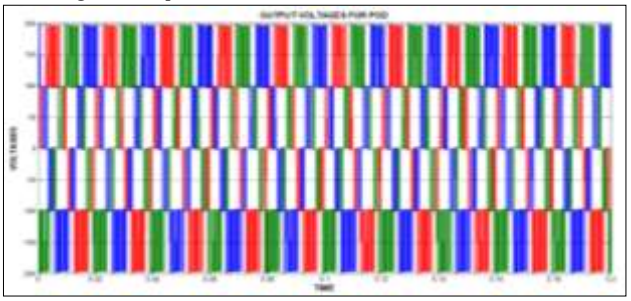

Fig. 15 Output Voltages for Three phase Open Loop Phase Opposition Disposition

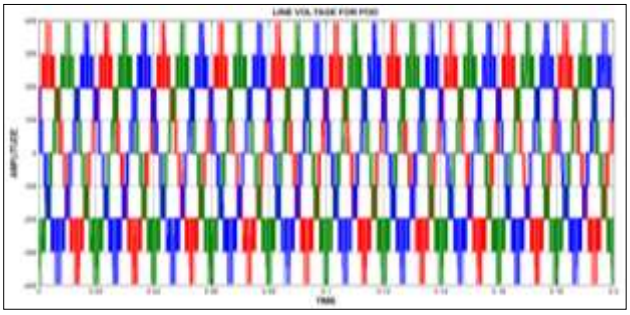

Fig. 16 Line Voltages for Three phase Open Loop Phase Opposition Disposition

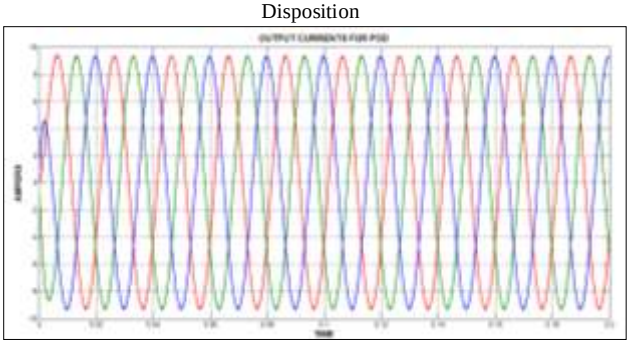

Fig. 17 Output currents for Three phase Open Loop Phase Opposition Disposition

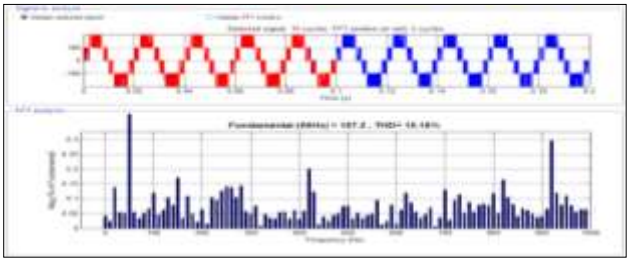

Fig. 18 % Voltage THD for Phase-A for Phase Opposition Disposition (%THD= 15.18)

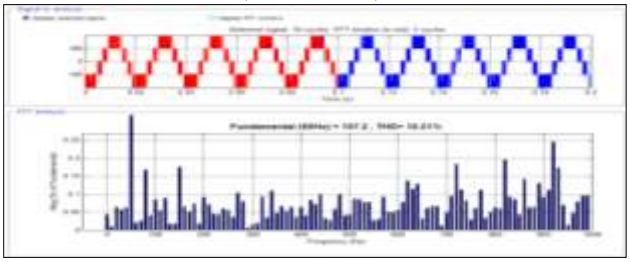

Fig. 19 % Voltage THD for Phase-B for Phase Opposition Disposition (%THD= 15.21)

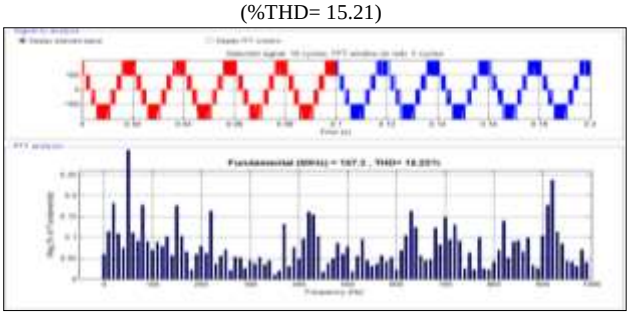

Fig. 20 % Voltage THD for Phase-C for Phase Opposition Disposition (%THD= 15.22)

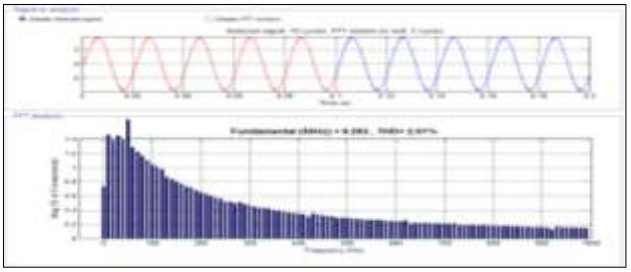

Fig. 21 % Current THD for Phase-A for Phase Opposition Disposition (%THD= 2.01)

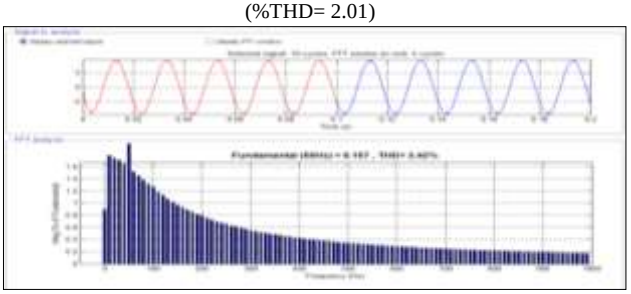

Fig. 22 % Current THD for Phase-B for Phase Opposition Disposition (%THD= 2.42)

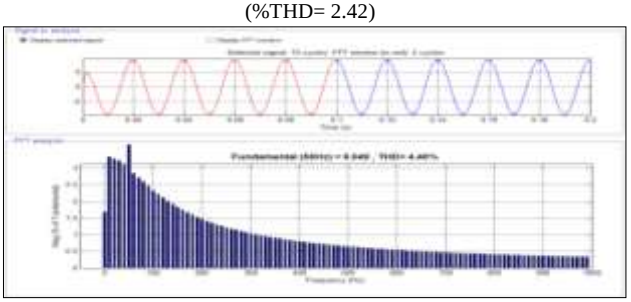

Fig. 23 % Voltage THD for Phase-C for Phase Opposition Disposition (%THD= 4.46)

Table 2.%THD analysis for Three Phase Open Loop Five Level CHB Inverter

	Modu. Index	Voltage THD (%)			Current THD (%)		
		Phase R	Phase Y	Phase B	Phase R	Phase Y	Phase B
THREE PHASE OPEN LOOP IPD	0.7	18.49	18.46	18.57	2.02	2.40	4.46
	0.8	15.23	15.12	15.19	1.99	2.41	4.45
	0.9	14.88	14.80	14.76	1.99	2.41	4.46
	1.0	**11.88**	**12.00**	**11.94**	**2.00**	**2.42**	**4.47**
THREE PHASE OPEN LOOP POD	0.7	18.78	18.69	18.75	2.03	2.43	4.47
	0.8	15.18	15.21	15.22	2.01	2.42	4.46
	0.9	15.00	15.04	15.04	2.00	2.42	4.47
	1.0	**11.95**	**11.90**	**11.87**	**2.00**	**2.42**	**4.47**
THREE PHASE OPEN LOOP	0.7	18.29	18.74	18.70	2.00	2.42	4.45
	0.8	15.23	15.21	15.14	2.00	2.42	4.46
	0.9	14.87	14.87	14.85	2.00	2.42	4.46
	1.0	**11.88**	**11.88**	**11.92**	**2.00**	**2.42**	**4.47**
APOD							

Simulink model and results of Single Phase Closed Loop Five Level Inverter for Alternate Phase Opposition Disposition:

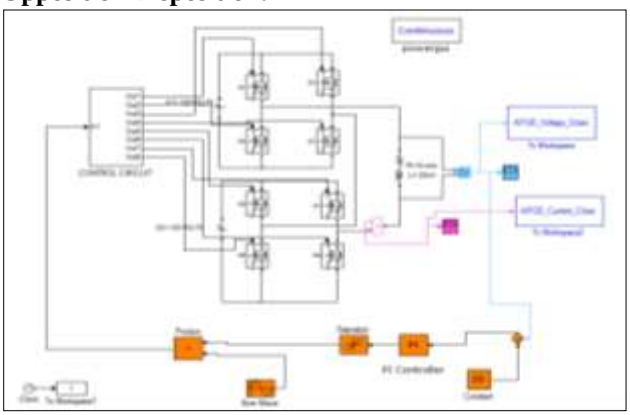

Fig. 24 Simulink model of Single phase Close Loop Alternate Phase Opposition Disposition

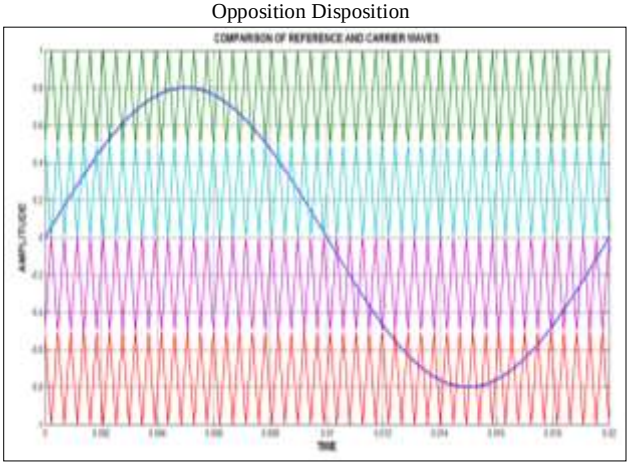

Fig. 25 Comparison of carrier and reference waves for APOD

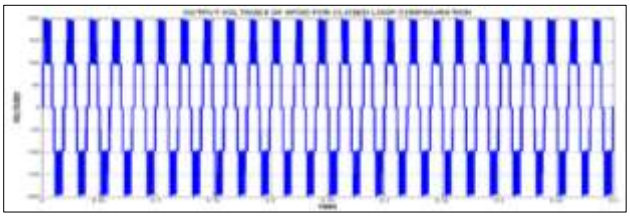

Fig. 26 Output Voltage of Single phase Close Loop Alternate Phase Opposition Disposition

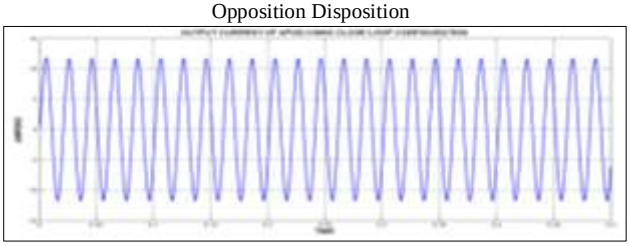

Fig. 27 Output Current of Single phase Close Loop Alternate Phase Opposition Disposition

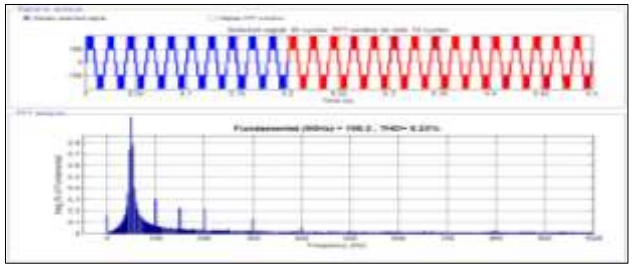

Fig. 28 %THD of Output Voltage for Single phase Close Loop Alternate Phase Opposition Disposition (%THD= 5.23)

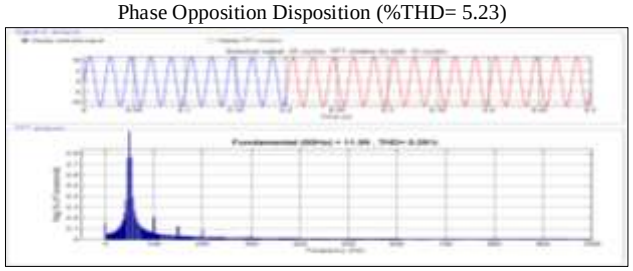

Fig. 29 %THD of Output Current for Single phase Close Loop Alternate Phase Opposition Disposition (%THD= 0.20)

Simulink model and results of Three Phase Closed Loop Five Level Inverter for In Phase Disposition:

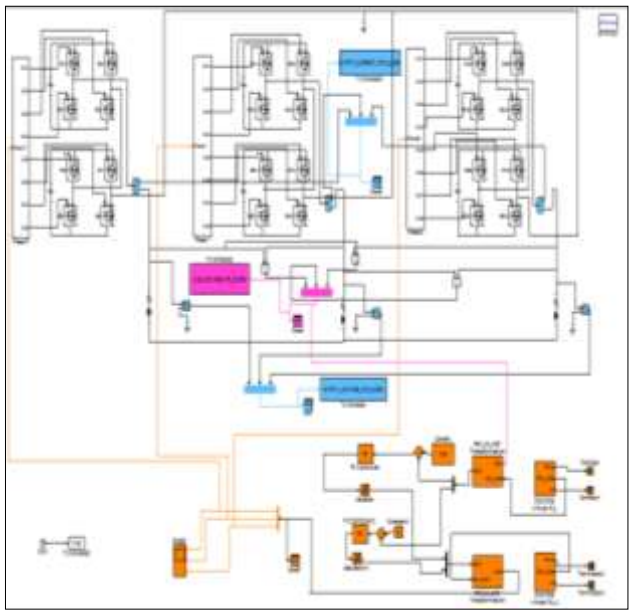

Fig. 30 Simulink model of Three phase Close Loop In Phase Disposition

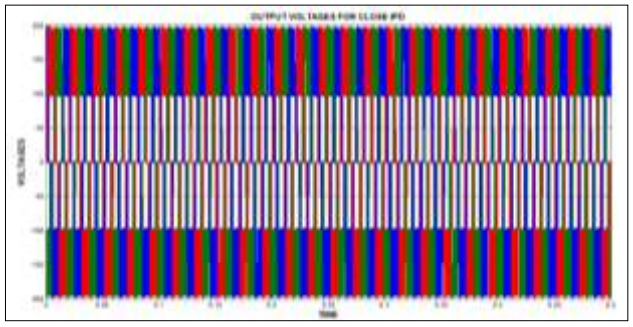

Fig. 31 Output Voltages for Three phase Close Loop In Phase Disposition

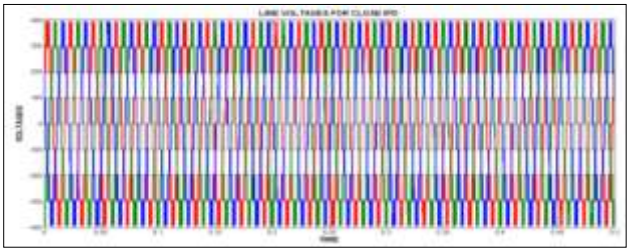

Fig. 32 Line Voltages for Three phase Close Loop In Phase Disposition

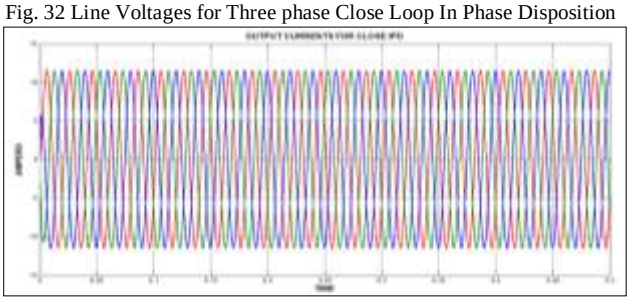

Fig. 33 Output Currents for Three phase Close Loop In Phase Disposition

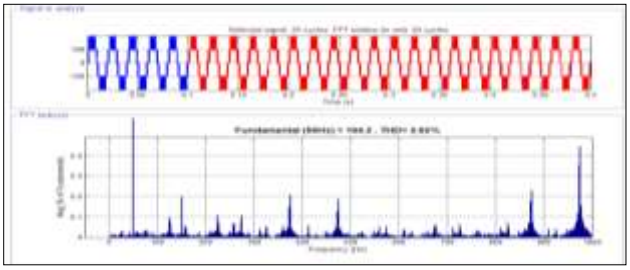

Fig. 34 % Voltage THD for Phase-A of Three phase close loop for In Phase Disposition (%THD= 2.62)

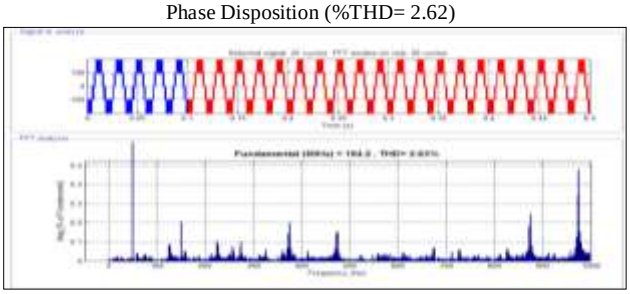

Fig. 35 % Voltage THD for Phase-B of Three phase close loop for In Phase Disposition (%THD= 2.63)

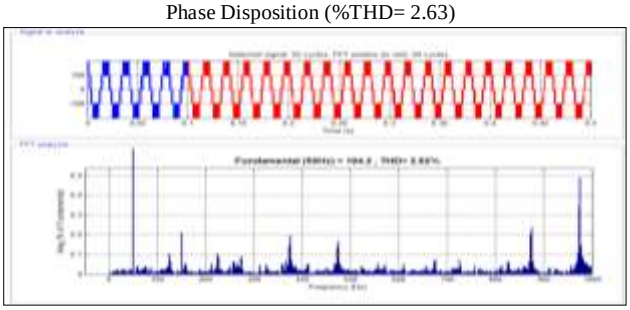

Fig. 36 % Voltage THD for Phase-C of Three phase close loop for In Phase Disposition (%THD= 2.62)

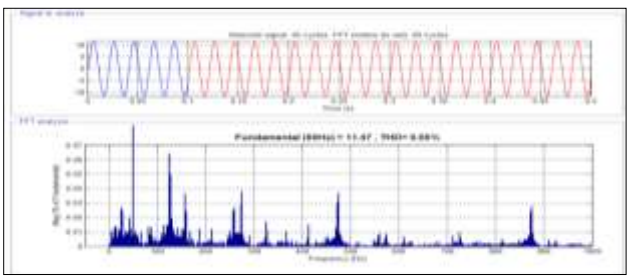

Fig. 37 Current THD for Phase-A of Three phase close loop for In Phase Disposition (%THD= 0.05)

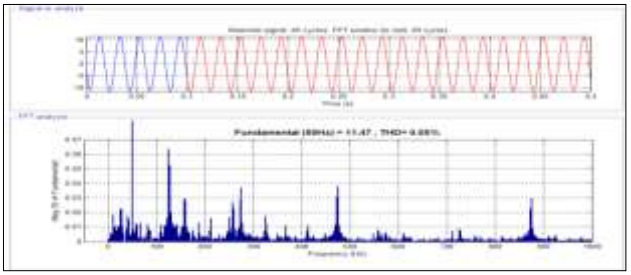

Fig. 38 Current THD for Phase-B of Three phase close loop for In Phase Disposition (%THD= 0.05)

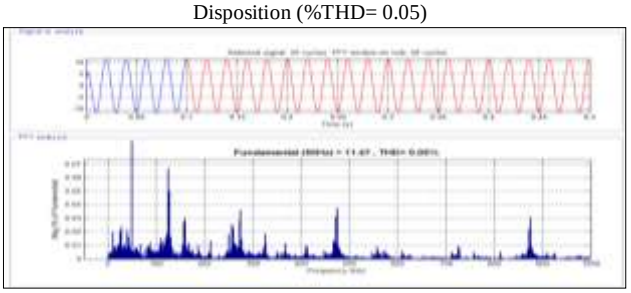

Fig. 39 Current THD for Phase-C of Three phase close loop for In Phase Disposition (%THD= 0.06)

V. COMPARATIVE RESULTS ANALYSIS

Table 3.Comparative results analysis for %THD of Single phase Open Loop and Close Loop Five Level CHB Inverter:

Modu. Index	Fund. Voltage	Voltage THD (%)	Current THD (%)	Fund. Voltage
	Open Loop IPD		**Closed Loop IPD**	
0.6	21.38	2.03	5.23	0.20
0.7	18.48	2.04	5.21	0.20
0.8	**15.18**	**2.00**	**5.23**	**0.20**
0.9	14.98	2.00	5.23	0.20
1.0	12.07	1.98	5.23	0.20
	Open Loop IPD		**Closed Loop IPD**	
0.6	20.98	2.04	5.26	0.19
0.7	18.43	2.03	5.23	0.19
0.8	**15.39**	**2.00**	**5.24**	**0.19**
0.9	15.12	1.99	5.24	0.19
1.0	12.15	1.97	5.24	0.19
	Open Loop IPD		**Closed Loop IPD**	
0.6	20.98	2.03	5.26	0.29
0.7	19.10	2.01	5.24	0.29
0.8	**14.94**	**2.01**	**5.23**	**0.29**
0.9	14.86	1.99	5.23	0.29
1.0	12.16	1.98	5.23	0.29

VI. CONCLUSION

The simulation of the Five Level Inverter for Single phase and Three-phase is successfully done using modulation topologies In-phase disposition (IPD), Phase opposition disposition (POD) and Alternate phase opposition disposition (APOD) method. The simulation results are carried out for Open loop and Closed loop configuration. %THD is measured for all three methods and %THD analysis is also carried out for the same methods. The comparative results analysis is also given for Open loop and Closed loop configuration. From the analysis it is concluded that among all three methods the APOD method is better. All the simulations are carried out in MATLAB/Simulink software. The results are taken at 0.8 modulation index and also for different modulation indexes (0.6-1.0) the results are also taken. For closed loop system, the results are taken at 1.0 modulation index and also for different modulation indexes (0.1-1.0) the results are taken. From the comparative results analysis it can be shows that the close loop system have better results than open loop system.

VII. FUTURE SCOPE

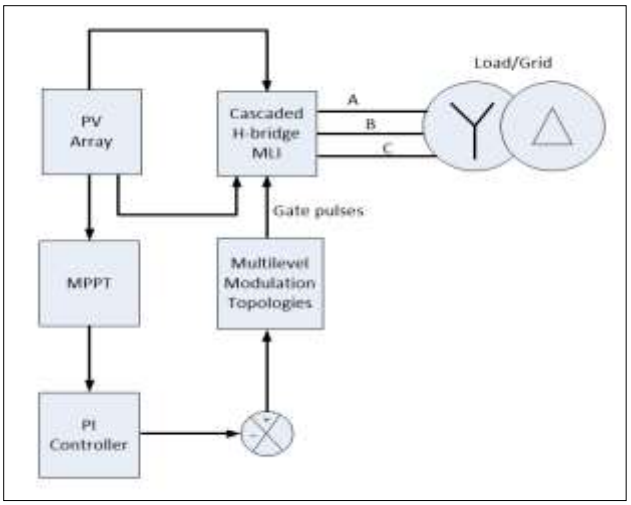

Fig. 40 Proposed topology connected with Grid

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