International Journal of Advance Research in Engineering, Science & Technology(IJAREST),
ISSN(O):2393-9877, ISSN(P): 2394-2444,
Volume 2, Issue 5, May- 2015, Impact Factor:2.125

Design of 16-bit Architecture for KLE Processor

Kanchan Joshi[1], Shruthi [2], Mohasinali Attar[3], Rahul Patil[4], Dr.U.V.Wali[5]

[1] *M.Tech VLSI, Dept. of ECE, KLE Dr. MSSCET Belagavi, India, kanchanj14@gmail.com*
[2] *M.Tech VLSI, Dept. of ECE, KLE Dr. MSSCET Belagavi, India, shruthimpatil5@gmail.com*
[3] *M.Tech VLSI, Dept. of ECE, KLE Dr. MSSCET Belagavi, India, mohasinaliattar@yahoo.co.in*
[4] *M.Tech VLSI, Dept. of ECE, KLE Dr. MSSCET Belagavi, India, rahul.pa86@gmail.com*
[5]*Professor, Dept. of ECE, KLE Dr. MSSCET Belagavi, India, udaywali@rediffmail.com*

Abstract

Design of a Microprocessor is a combination of many combinational and sequential circuits. The present paper describes the modules such as datapath, ISA, clock system and memory unit's design and implementation for the microprocessor design work being taken up at the college level. The need of today's VLSI technology is to implement all the modules with less power consumption and high speed operation. The proposed architecture is the design and implementation of 16-bit Processor using Verilog HDL and Cadence tools for the design of Processor undertaken by the students. At KLE Dr. MSSCET College, a project has been envisioned to develop a microprocessor from the architectural to physical level implementation. A RISC based Von-Neumann architecture design of KLE microprocessor is developed.

Keywords- *6T SRAM, , RISC, Program Counter, ISA, PLL, Cadence Tool, Xilinx.*

I. INTRODUCTION

A microprocessor incorporates the different functionality modules of any general purpose or application specific embedded system. Microprocessors are multipurpose programmable devices. They accept digital data input, processes it according to the instructions stored in its memory and produces output. These are the sequential digital logic modules, as they possess internal memory operating on binary numbers.

Arithmetic and Logical Unit (ALU) is essentially a digital module performing all the operations, depending on the selection bits ALU executes the appropriate operations. Along with ALU output there are also status bits which represent exception in the arithmetic operations. They are result zero, overflow, and divide by zero and other basic operation. The selection unit mainly consists of multiplexers. The design includes the datapath for a CPU containing Program Counter (PC), Memory Address Register (MAR), Memory Data Register (MDR), Instruction Register (IR), Register File (RF) and other various components to tie them all together. [1].

A. DATAPATH AND ISA

A Von Neumann Architecture was the revolutionary idea of John von Neumann to merge the data memory and instruction memory. This made it possible to treat program code as data and to perform operations on it. This was, for example, used for adding an array of numbers stored in consecutive memory cells, typically performed by a tight program loop. It uses a single memory for both instructions and data [1].

For any new microprocessor design, ISA and Datpath design is essential. Instruction Set Architecture specifies the number of instructions, instruction format, type of the operands and type of the operation to be performed. Datapath is responsible for the execution of all the operations performed by the microprocessor. Design of the datapath is to define the path for each executable part. But datapath cannot perform the operations unless it obtains the signals from controller to perform the required action [2].

B. MEMORY

The memory is widely used in embedded system and many Electronic device to store the data and program. The authors Amith Singhee claim that "Much of the VLSI design effort across the industry is spent on designing memories. These include static random access memory (SRAM), dynamic RAM (DRAM), embedded DRAM, and non-volatile memories (NVM) like NOR flash. These memories are typically arrays of millions of memory cells. We refer to circuits, such as these memory cells, as High-Replication Circuits (HRCs) because they have the unique feature of being highly replicated in a single die. Other circuits like latches and flip-flops also fall in this class of HRCs, now that we may see millions of instances of a latch in an aggressive multi-core microprocessor. An increasingly difficult aspect of designing these HRCs is meeting the extremely high parametric yields required for them. The high yield requirement is imposed by their high (and increasing) replication count."(p.p 2-3) [7]

In this paper we purposed new 6T SRAM cell which we have designed and compared with conventional 6T SRAM cell.

C. GENERAL ARCHITECTURE OF CLOCK SYSTEM

The below figure represents a generalized structure of clock system. It consists of parts like:

1. Phase locked loop
2. Buffers

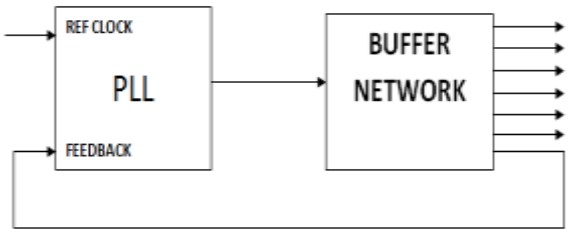

Figure 1: Block diagram of clock distribution[3]

A microprocessor consists of many sequential and combinational circuits. In addition to these it consists of circuits which act as storage elements. All these circuits are interdependent on each other. Hence they should work in synchronous with each other. A system is required which ensures this. Clock system ensures working and in particular synchronized working of all the circuits. A good clock system design ensures that there is zero or minimal clock skew and also the clock signal should have low jitter and noise. The important part or the essence of the clock system is the phase locked loop. Over the years with the demand for more accurate, fast and less noise conditions have led to a drastic change in the design of phase locked loops from purely analog to purely digital in nature.

As the complexity and processing capability of the Processor increases designers face the problem of providing a good and efficient clock system.

II. PROPOSED DESIGN OF MODULES

A. ARCHITECTURE INSTRUCTION SETS AND DATAPATH

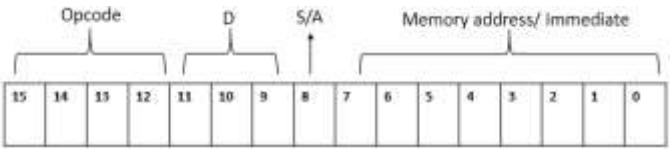

Figure 2: Instruction Format.

Figure 2 shows the instruction set format for the proposed design and implementation of 16-bit ALU for KLE processor. Here 0-7 bits are reserved for memory address/immediate, 8th bit is the source address bit that is accumulator bit since our proposed datapath design is accumulator based architecture. 9-11 bits are destination address bits and 12-15 MSB bits are reserved for opcode of the instruction. Bits 8-11 can be utilized as source destination bits or as opcodes depending upon the type of instruction and its operation on registers. Hence the design can be further extended to have more than 16-instructions.

The details in the table gives the instructions that are being implemented for the design of ISA. The operations of each instructions is shown with the register transfer level. The opcode for each of the instruction can be decoded in accordance with the offsets determined by the decoder unit.

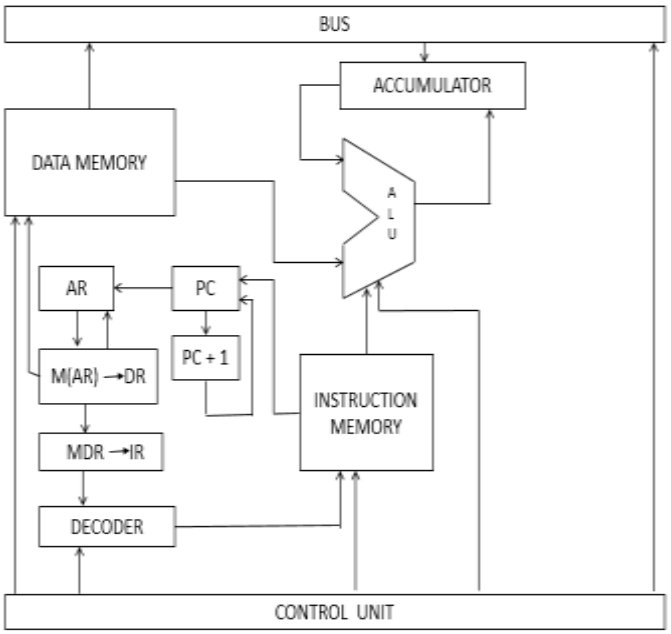

Figure 3: Datapath Architecture.

In our proposed methodology, datapath architecture is based on the accumulator based architecture as shown in figure 3. Here one of the operand register is always accumulator and another operand is from any of the registers or from the address of the memory. Datapath is responsible for the actual execution of all the operations. Datapath actions are enabled by the control unit signals which are set or reset depending upon the flags and conditional operations. For each of the stages of execution it will be in the standby with the corresponding data ready for a particular action to be executed. MAR and MDR are the registers holding the data or address during these intermediate levels.

B. MEMORY ARCHITECTURE

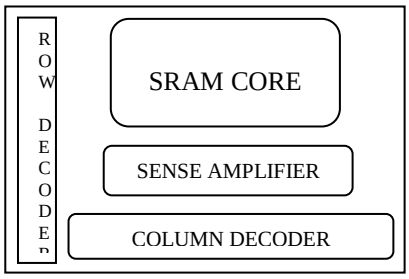

Figure 4: Memory Architecture

The figure 4 shows the block diagram of SRAM memory architecture. It consists of SRAM Core, Sense amplifier, Row Decoder and Column Decoder.

OPCODE[15:9]			INSTRUCTION	OPERATION	RTL OPERATION
BINARY	D	S			
0000	000	0	NOP	No operation	PC ← PC
0000	000	S	LOAD X	Load the contents of address X into accumulator	ACC ←X
0000	001	S	NOT	Compliment the contents of accumulator	ACC ← ~(ACC)
0001	D	S	MOV X	Move the contents of accumulator into register	X ←ACC
0010	D	S	ADD X	Add the contents of address X to accumulator and store the result in accumulator	ACC ← ACC + X
0011	D	S	SUB X	Subtract the contents of address X from accumulator and store the result in accumulator	ACC ←ACC - X
0100	D	S	MUL X	Multiply the contents of address X with the contents of accumulator and store the result in accumulator	ACC ← ACC * X
0101	D	S	DIV X	Divide the contents of accumulator by the contents of address X and store the result in accumulator	ACC ← ACC / X
0110	D	S	CMP X	CMP the contents of address X with accumulator and store the result in accumulator	ACC←ACC CMP X
0111	D	S	NAND X	NAND the contents of address X with accumulator and store the result in accumulator	ACC ←~(ACC & X)
1000	D	S	NOR X	NOR the contents of address X with accumulator and store the result in accumulator	ACC ←~(ACC & X)
1001	D	S	AND X	AND the contents of address X with accumulator and store the result in accumulator	ACC ← ACC & X
1010	D	S	OR X	OR the contents of address X with accumulator and store the result in accumulator	ACC ← ACC | X
1011	D	S	XOR X	XOR the contents of address X with accumulator and store the result in accumulator	ACC ← ACC ^ X
1100	D	S	SHL ACC	Shift left the contents of accumulator	ACC<<
1101	D	S	SHR ACC	Shift right the contents of accumulator	ACC >>
1110	D	S	JC	Jump if carry flag is set	PC ← [OFFSET]
1111	D	S	JZ	Jump if zero flag is set	PC ← [OFFSET]

Table 1: Instruction set

i. MEMORY OPERATION

A) Six-Transistor (6T) CMOS SRAM Cell

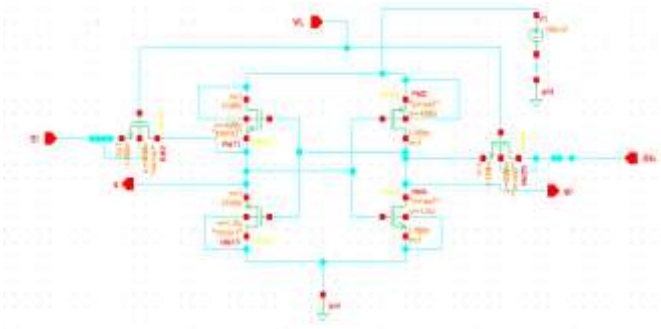

Figure 5: Six Transistor SRAM cell

The six transistor (6T) CMOS SRAM cell is shown in figure 5. It consists of two pMOS pull-up transistors Q3, Q4, access transistors *Q5* , *Q6 and pull down nMOS Q1, Q2*.. The gate terminal of Q5 and Q6 transistors are connected to word line. The transistor Q5 and Q6 provides read and write access to the cell. In this circuit pull down NMOS transistors *Q1* and *Q2* are used to store the bit.

B) READ OPERATION

During read operation the BL=1, BLB=1 and WL=1 lines are charged to VDD or high. During read cycle bit-bar signal will goes low and the sense amplifier sense the bit from SRAM Cell through YMUX column circuitry. The sense amplifier consumes very less power during the read operation.

C) WRITE OPERATION

To write one in SRAM cell the bitlines and wordline WL should be at state of BL=1,BLB=0 and WL=1. During this cycle the write circuitry store the bit in SRAM memory cell through the access transistor Q5 and Q6.

To write 0 in SRAM cell the bitlines and wordline WL should be at state of BL=0, BLB=1 and WL=1. During this cycle the write circuitry store the bit in SRAM memory cell through the access transistor Q5 and Q6.

ii. SRAM 1 BIT MEMORY CELL AND TEST CIRCUIT

Figure 6 and 7 shows the implementation of 1-bit full stack SRAM memory schematic and test circuit.

iii. RESULT OF 1BIT SRAM CELL

Simulation of 1 bit SRAM cell is done on cadence environment. We can see the result of write and read operation of SRAM cell.

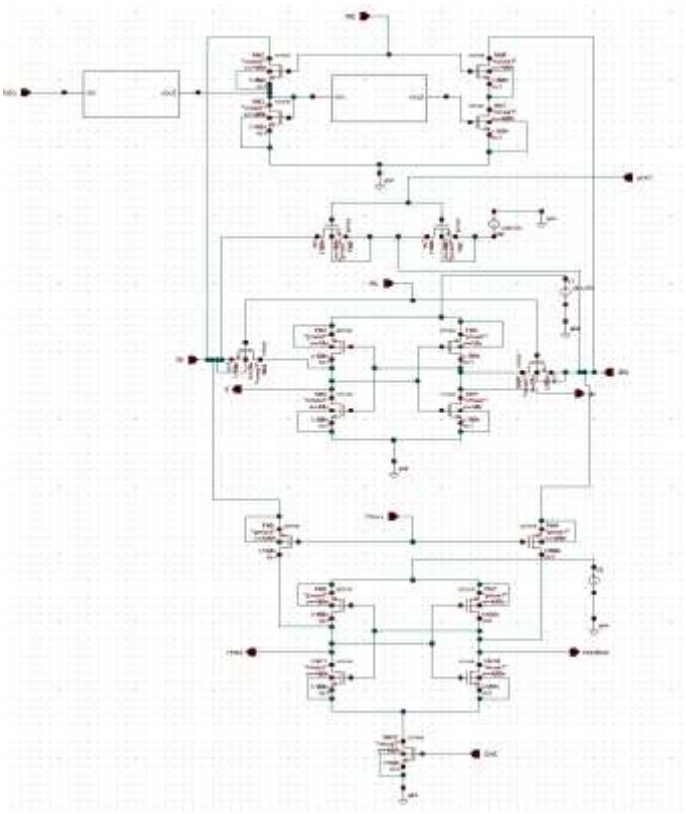

Figure 6: Full Stack of SRAM cell

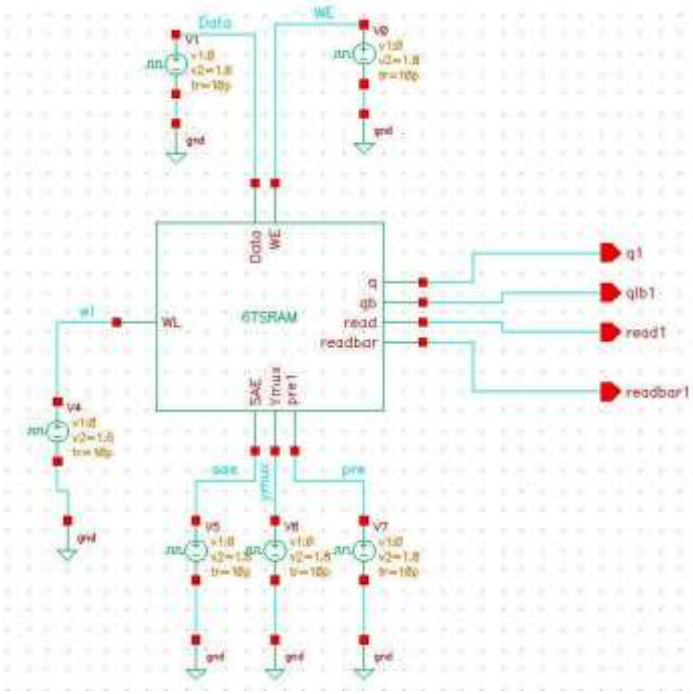

Figure 7: Test Circuit of SRAM full Stack

WRITE O:

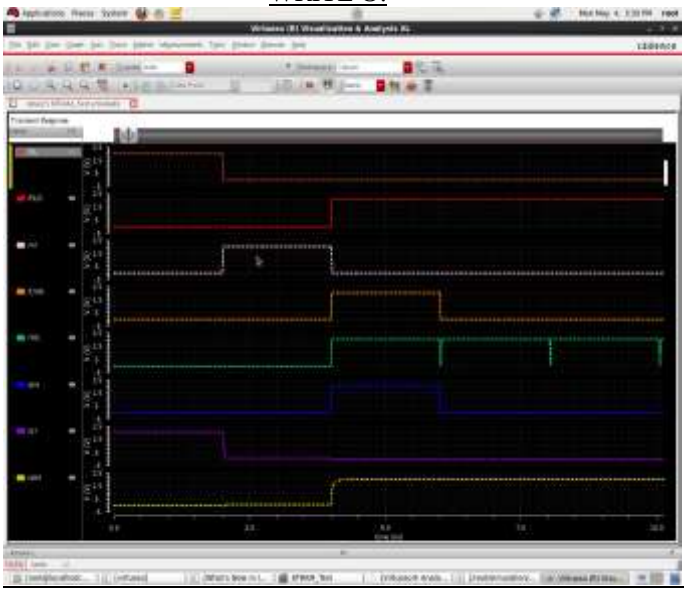

Figure 8: waveform of write zero

WRITE 1:

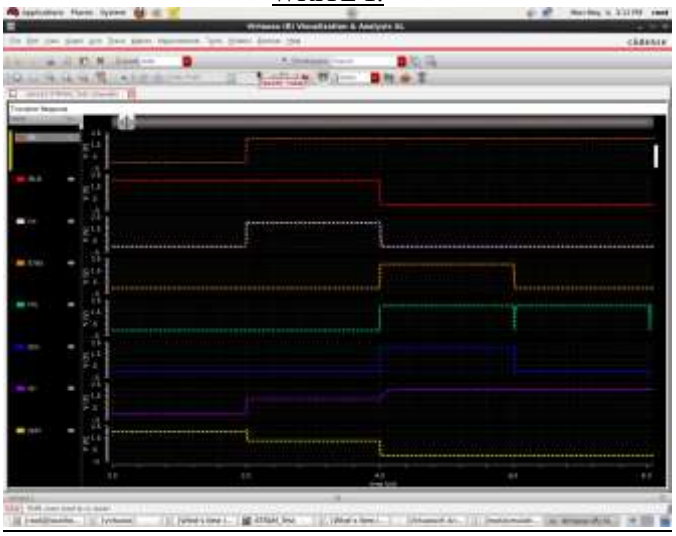

Figure 9: Waveform of write 1

READ WAVEFORM

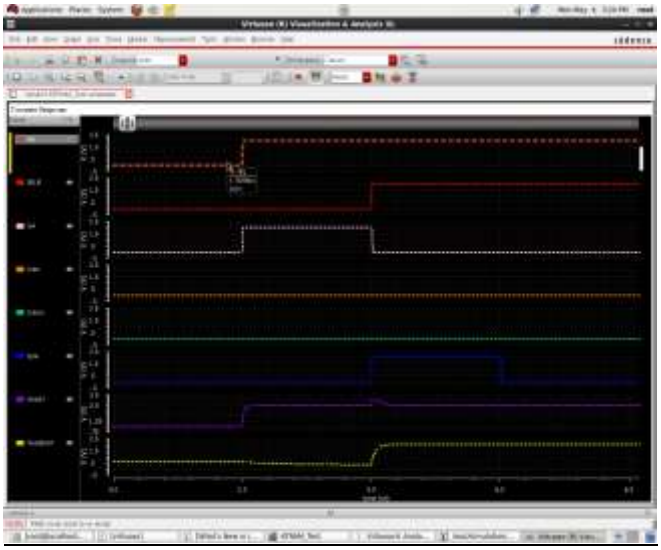

Figure 10: SRAM Read

C. CLOCK SYSTEM FOR KLE PROCESSOR

Since the initial phase of development of the processor involves the implementation of a instruction set architecture (ISA) and a memory unit, the clock system required for the distribution would be not so complex. Hence the type of distribution topology required at this stage would be as shown in the fig. below. In future as the development of the processor expands beyond the present modules, a different topology would be required. To achieve this, the block diagram of fig. can be easily modified to suit the requirements. Also the essence of the clock system i.e. PLL can be redesigned with enhanced specifications to address the increased complexity. The below figure 10 represents block diagram of the proposed clock system for the KLE processor.

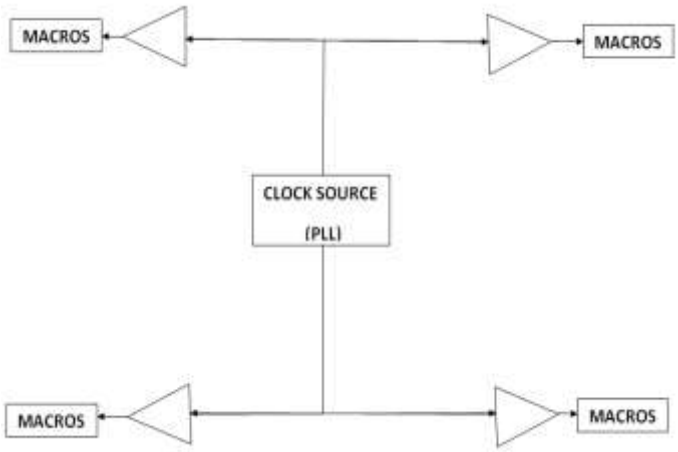

Figure 10: Block diagram of Clock distribution topology[4]

D. PHASE LOCKED LOOP

Phase locked loop is a closed loop feedback system that consists of phase detector, filter and a controlled oscillator. Phase detector compares the reference signal and the feedback signal and generates phase error. Based on this phase error the oscillator either increases or decreases the oscillation frequency. PLL along with buffers help in

achieving zero clock skew for a clock system. The below table gives the differences between the various types:

PLL CATEGORY	PHASE DETECTOR	PHASE ERROR SIGNAL	LOOP FILTER
LINEAR PLL	ANALOG	ANALOG	ANALOG
DIGITAL PLL	DIGITAL	ANALOG	ANALOG
ALL DIGITAL PLL	DIGITAL	DIGITAL	DIGITAL
SOFTWARE PLL	SOFTWARE	SOFTWARE	SOFTWARE

Table 2.: Different categories of PLL[5].

Traditionally the phase locked loop consisted of all analog signals. A phase detector is used to detect any phase difference (also difference in frequency) with respect to the reference signal (which is a signal from clock source) and the feedback signal. The phase detector is followed the loop filter. The output of the loop filter operates the oscillator. Hence the oscillator employed here is known as the voltage controlled oscillator (VCO).
Here in the present case, owing to the lesser number of modules traditional analog phase locked loop is being employed. The analog phase locked loop also known as linear phase locked loop consists of the following parts:

1. Phase frequency detector
2. charge pump and low pass filter
3. voltage controlled oscillator
4. Frequency divider (Optional)

The below figure 11 represents the block diagram of the phase locked loop being used in the present design of the proposed clock system.

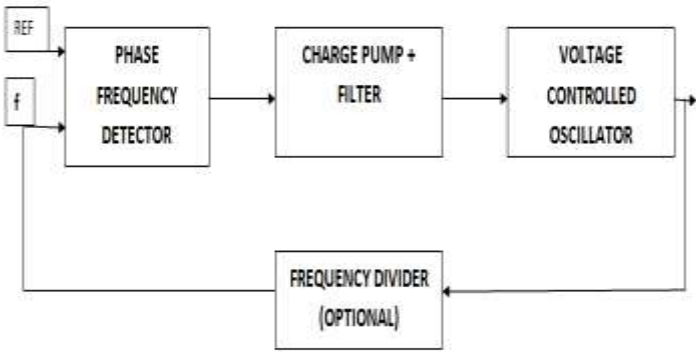

Figure 11: Block diagram of PLL [3]

III.CONCLUSION

The paper presents implementation of each module of the proposed processor architecture. The implementation of memory, datapath, ISA and clock system and their schematic and RTL views in cadence and Xilinx tools have been shown and the results obtained are satisfactory to proceed further for the integration with all other modules.

REFERENCES

[1] Enoch O. Hwang - "Microprocessor Design", Principles and Practices With VHDL.

[2] Miles J. Murdocca, Vincent P. Heuring,"Principles of computer architecture", class test edition – august 1999.

[3] www.wikipedia.org/wiki/Phase-locked_loop

[4] "Clocking in Modern VLSI Systems", Thucydides Xanthopoulos Editor, Springer 2009.

[5] R. E. Best, *Phase Locked Loops Design Simulation and Applications*, McGraw-Hill Professional, 5th Edition, 2003.

[6] Design and Physical Implementation of Asymmetric 8T-SRAM Memory Systems - The International Journal Of Engineering And Science (IJES) ||Volume||2 ||Issue|| 7 ||Pages|| 35-41||2013|| ISSN(e): 2319 – 1813 ISSN(p): 2319 – 1805.

[7] Extreme Statistics in Nanoscale Memory Design by Amith Singhee and Rob Rutenbar. Pages|| 2-3||

[8] Design and Physical Verification of Low Power 4words X 4bits SRAM System using an Adaptive Voltage Level (AVL) Technique by Kumaraswamy N1, Mahesh B Nelagar, International Journal of Advanced Research in Computer and Communication Engineering Vol. 3, Issue 6, June 2014

[9] Monika Yadav, Shyam Akashe, Yogesh Goswami, " Analysis of leakage reduction techniques on different SRAM cells,"International Journal of Engg. Trends and Tech., vol.2, issue 3, pp.78-83, 2011.

[10] CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies By Andrei Pavlov. (Pages.26,30)

[11] Yamin Li and Wanming Chu "Aizup - A Pipelined Processor Design and Implementation on XILINX FPGA Chip", FCCM'96, IEEE Symposium on FPGAs for Custom Computing Machines, April 17 – 19, 1996, Napa, California, USA, pp.98–106.

[12] Jinde Vijay Kumar, Boya Nagaraju, Chinthakunta Swapna and Thogata Ramanjappa, "Design and Development of FPGA Based Low Power Pipelined a64-Bit RISe Processor with Double Precision Floating Point Unit", International Conference on Communication and Signal Processing, April 3-5, 2014, India