Impact Factor (SJIF): 3.632

International Journal of Advance Research in Engineering, Science & Technology

e-ISSN: 2393-9877, p-ISSN: 2394-2444

(Special Issue for ITECE 2016)

A Novel PWM Technique to Reduce Common Mode Voltage in Coupled Inductor Multilevel Inverter

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Abstract --- *This work presents multi-carrier interleaved PWM strategies to control common mode voltage in three phase coupled inductor inverter (CII). The proposed scheme has the advantages of reduced number of switches with higher output voltage level. The common problem arise in the coupled inductor inverter (CII) is the inductor power losses that are related to the magnitude of current ripple. The proposed multi-carrier interleaved PWM scheme technique is easily to implement when compared to other PWM techniques, and also one of the advantage to minimize the inductor current ripple. The minimization of the current ripple leads to the reduction in the common mode current participation in the (Y-Δ) connected induction motor. The common mode voltage that is the integration of the common mode current in each phase. The multi-carrier interleaved consists of the continuous and discontinuous modes of operation. By choosing the proper high effective winding inductance switching state (DPWM) can reduce the Common mode voltage without degrading the performance of the inverter. The proposed scheme is applied for three-phase coupled inductor inverter to obtain the five level output. Mathematical analysis & Simulation studies are verified in Mat lab 2012b.*

Keywords --- *Coupled Inductor Inverter, Common Mode Voltage and PWM Techniques.*

I. INTRODUCTION

In high power and high voltage two level inverter have some limitation in operating at high frequency mainly due to switching loss [5]. Where the multilevel inverter presents a new set of feature that are well suited for use in reactive power compensation and it may easier to produce a high power, high voltage inverter with multilevel structure because voltage stresses are controlled in the structure. Increasing the number of voltage level in the inverter without requiring higher rating on individual devices can increase the power rating. In multilevel inverter as the number of voltage level increases the harmonics content of the output voltage waveform decreases significantly.

Concept of multilevel inverter is derived from three phase inverter system. Series connected capacitor constitute the energy bank for inverter and provides to obtain to the different step output voltage in MLI. The term level is referred to as the number of capacitor banks and banks energy all used by switches. The phase output voltage can be defined as the voltage across output terminals of the inverter and the ground point.

The topological structure of multilevel inverter should have less switching devices as far as possible, capable of withstanding very high input voltage for high power application, lower switching frequency for each switching device.

PWM based inverter has been widely applied to many ac motor drives, a number of problem such as motor bearing damage, electromagnetic interference, breakdown of winding insulation, and motor leakage current have been a raised. Due to that CMV a raised in the system, Multilevel Inverter generates an alternating common mode voltage at the motor terminals and this cause’s unwanted current produces and motor failure. To solve this problem choke is connected to system open end induction motor different PWM techniques are used.

To overcome this problem the one of the most advantage techniques by increasing the level of output and selecting the proper switching state to operate in the low CMV can be elaborated.

Research Objective:

To achieve improvement in the efficiency and performance of the CII topology as main objective is the current ripple should be carefully considered, and the impacts of different factors on minimizing ripple should be examined.

The objectives of this project can be categorized as follows:

1. Analysis the factors that contribute to the winding current and output Current ripples in the CII topology.
2. Develop a suitable PWM switching scheme which minimizes the high frequency Current ripples and allows for operation over a wide range modulation amplitudes.

3. Improve the CII inverter performance with drives by
    a. Minimizing the inductor losses associated to high frequency current ripple.
    b. Reducing the CMV by maintaining the proper switching state in the CII fed drives.

II. PULSE-WIDTH MODULATION TECHNIQUES

The energy that a switching power converter delivers to a motor is controlled by Pulse Width Modulated (PWM) signals applied to the gates of the power transistors. PWM signals are pulse trains with fixed frequency and magnitude and variable pulse width. There is one pulse of fixed magnitude in every PWM period. However, the width of the pulses changes from pulse to pulse according to a modulating signal. When a PWM signal is applied to the gate of a power transistor, it causes the turn on and turn off intervals of the transistor to change from one PWM period to another PWM period according to the same modulating signal. The frequency of a PWM signal must be much higher than that of the modulating signal, the fundamental frequency.

Types of PWM Techniques:
The efficiency parameters of a multilevel inverter such as switching losses and harmonic reduction are principally depended on the modulation strategies used to control the inverter. As depicted in multilevel inverter control techniques are based on fundamental and high switching frequency. Another widely used popular classification for the modulation methods developed to control the multilevel inverters is depend upon open loop and closed loop concepts as depicted. Three main control techniques of multilevel inverters are SHE-PWM, PWM, and optimized harmonics stepped pulse width modulation (OHS–PWM). The regular PWM modulation method can be classified as open loop and closed loop owing to its control strategy. The open loop PWM techniques are SPMW, space vector PWM, sigma–delta modulation, while closed loop current control methods are defined as hysteresis, linear, and optimized current control techniques. The modulation methods developed to control the multilevel inverters are based on multi-carrier orders with PWM. Due to pre-defined calculations are required, SHE-PWM is not an appropriate solution for closed loop implementation and dynamic operation in multilevel inverters. Among various control Schemes, the sinusoidal PWM (SPWM) is the most commonly used control scheme for the control of multilevel inverters. In SPWM, a sinusoidal reference waveform is compared with a triangular carrier waveform to generate switching sequences for power semiconductor in inverter module.

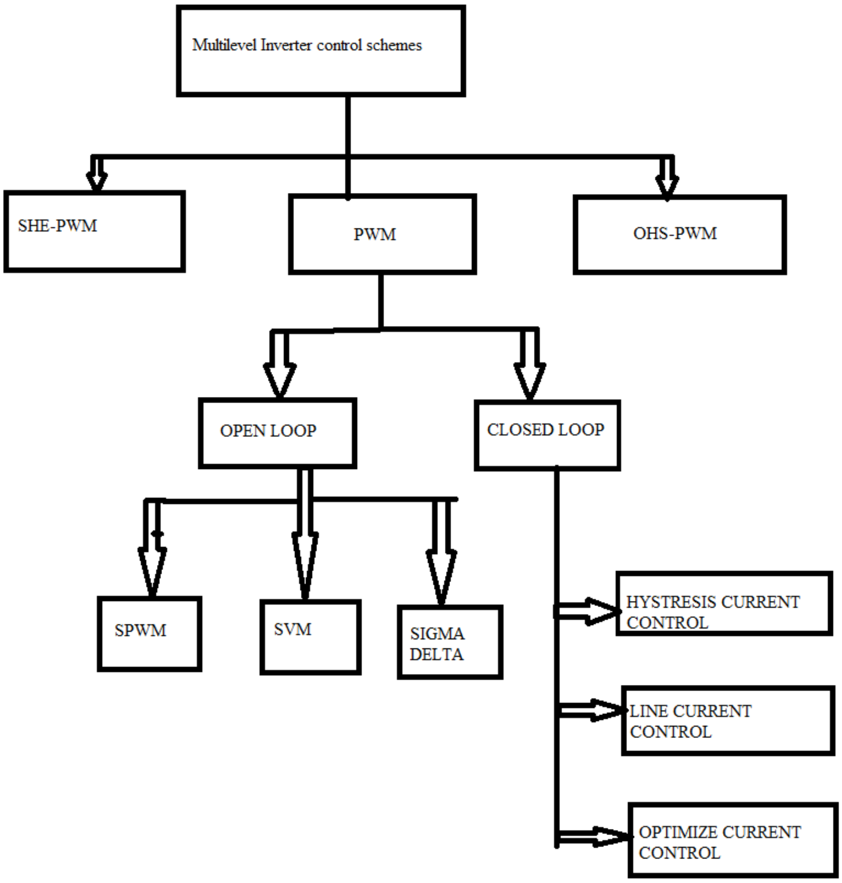

Figure.1. Different PWM Techniques

III. THREE PHASE THREE LEVEL INVERTER WITH COUPLED INDUCTOR

Operation Of Coupled Inductor Inverter (CII):

From the figure 2 shows the proposed topology of three levels NPC with coupled inductor configuration consists of the lower and the upper switches. Here both the upper and lower switches are interconnected with the lower and upper windings to obtain the extra voltage level in the output. The inverter leg is A consist of four active switches S1, S2, S3 and S4, two clamping diodes connected to the neutral point and two free wheel diodes connected to the DC bus at + and – points. Each leg in the inverter consists of N number of switches.

The possible switching states can be declared as N^2, for example in this case 16 states in one leg. In the total switching states possible in the overall inverter is given as the $(N^2)^P$, P represent the phase available in the inverter. So totally 4096 possible states for four switch three phase structure, The pole voltage produced by the coupled inductor in each leg will consist of 0,+ ¼ V_{dc}, ,+ ½ V_{dc}. Compare to the standard NPC state here extra level voltages are induced that are + ¼ Vdc. From the figure.3 shows the operation of the coupled inductor and output voltage of each level.

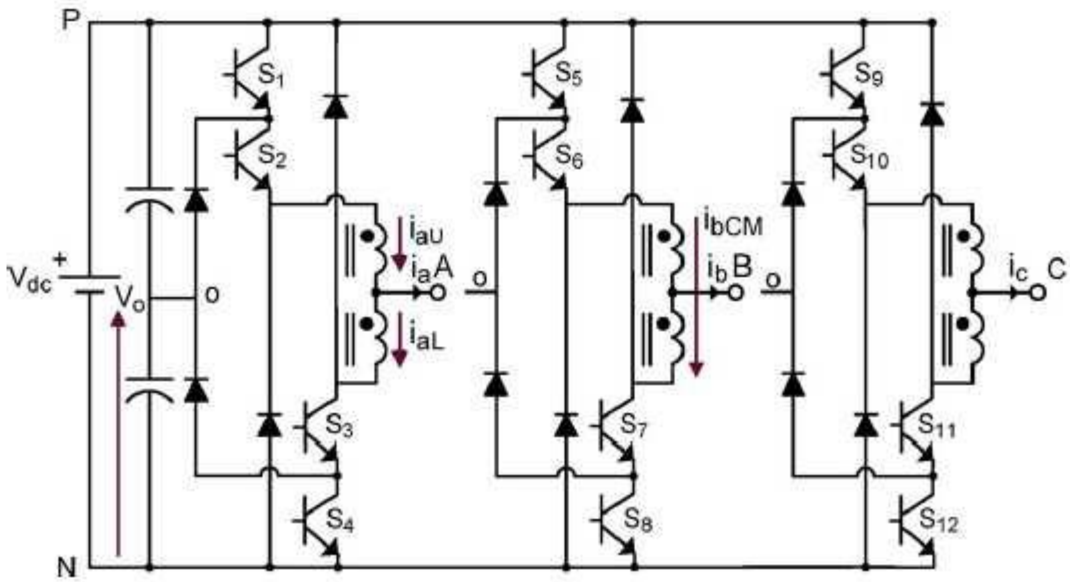

Figure.2. Five level NPC Inverter topology using a three phase coupled inductor

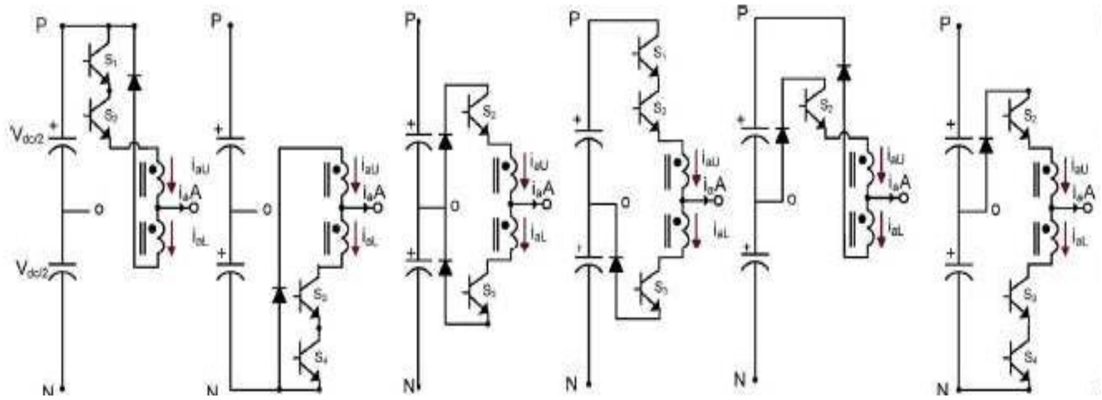

Figure.3. Different modes of operation of 3-level NPC-CII

Analysis of Inverter with Switching States:

The influence of switching operation in the inverter can impact on the inductor common mode current is represented in table 1. The inductor winding is short circuit in the normal operating condition of the inverter at that condition the common mode DC current is maintain at constant it is shown in figure 3. However by applying state that can make the positive charging of the inductor it will produce the pole voltage of range +1/4 Vdc at this operation the common mode

DC current increase and going for the positive discharging the common mode DC current decrease. In the above both conditions the common mode DC current is not maintained constant it will lead to influence of the neutral point balancing in the inverter.

Table.1. Switching type of the coupled inductor inverter

Switching Type	S 1	S 2	S 3	S 4	Inverter Pole Voltage	Coupled Inductor Winding	Common Mode DC Voltage
Positive	1	1	0	0	$+1/2V_{dc}$	Short Circuit	Maintains
Positive Charging	1	1	1	0	$+1/4V_{dc}$	Charging Mode	Increase
Positive Discharging	0	1	0	0	$+1/4V_{dc}$	Discharging Mode	Decrease
Zero	0	1	1	0	0	Short Circuit	Maintains
Negative Charging	0	1	1	1	$-1/4V_{dc}$	Charging Mode	Increase
Negative Discharging	0	0	1	0	$-1/4V_{dc}$	Discharging Mode	Decrease
Negative	0	0	1	1	$-1/2V_{dc}$	Short Circuit	Maintains

Common Mode Voltage:

The common mode voltage is measured between the inputs of the voltage source rectifier to the star connected load. It is defined as,

$$\mathbf{V_{NG} = (V_{AN}+V_{BN}+V_{CN})/3}$$

Effect of CMV:

The common mode voltage generated by an inverter is defined as the voltage between apparatus neutral and its ground e.g. in case of an AC drive it is the stator neutral and the system ground. The common mode voltage is the sum of the three phase voltages of the inverter with respect to ground. In any PWM technique the output of every phase is in the form of pulses. Due to this, the common mode voltage also consists of high frequency voltage pulses of certain magnitude which appears between the application neutral and the ground. The common mode voltage leads to common mode current in the system.

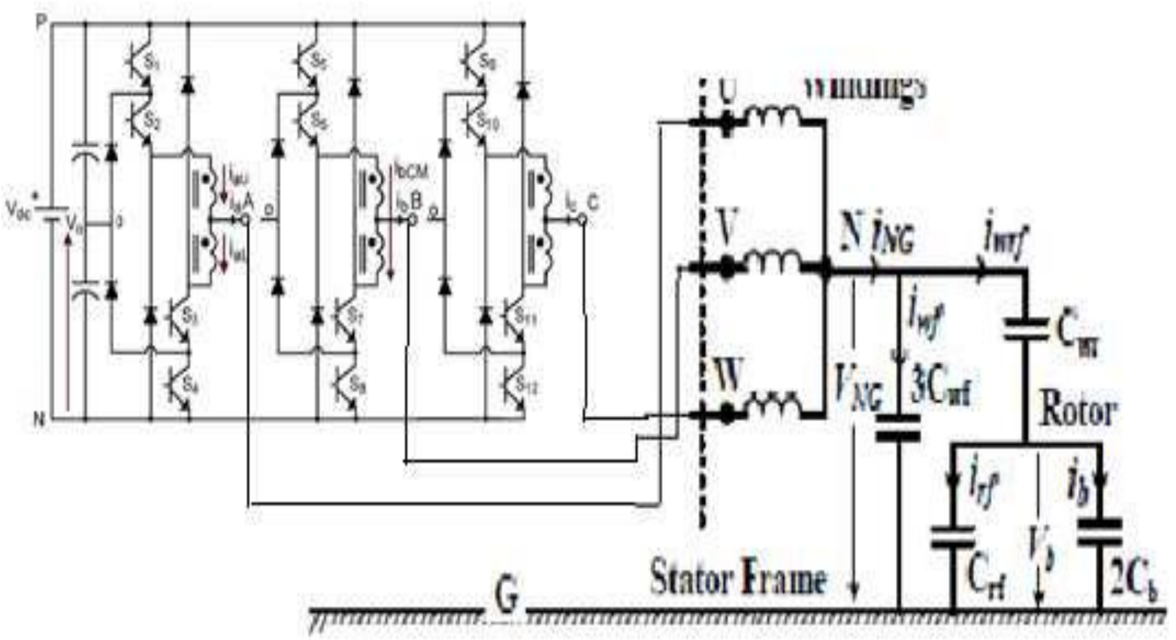

Figure.4. Circuit layout of CII and motor system

IV. SIMULATION RESULTS AND DISCUSSIONS

In this, the output results are summarized and analyzed based on the discontinuous pulse width modulation technique and also phase disposition and phase opposition disposition.

Simulation of Coupled Inductor Inverter:

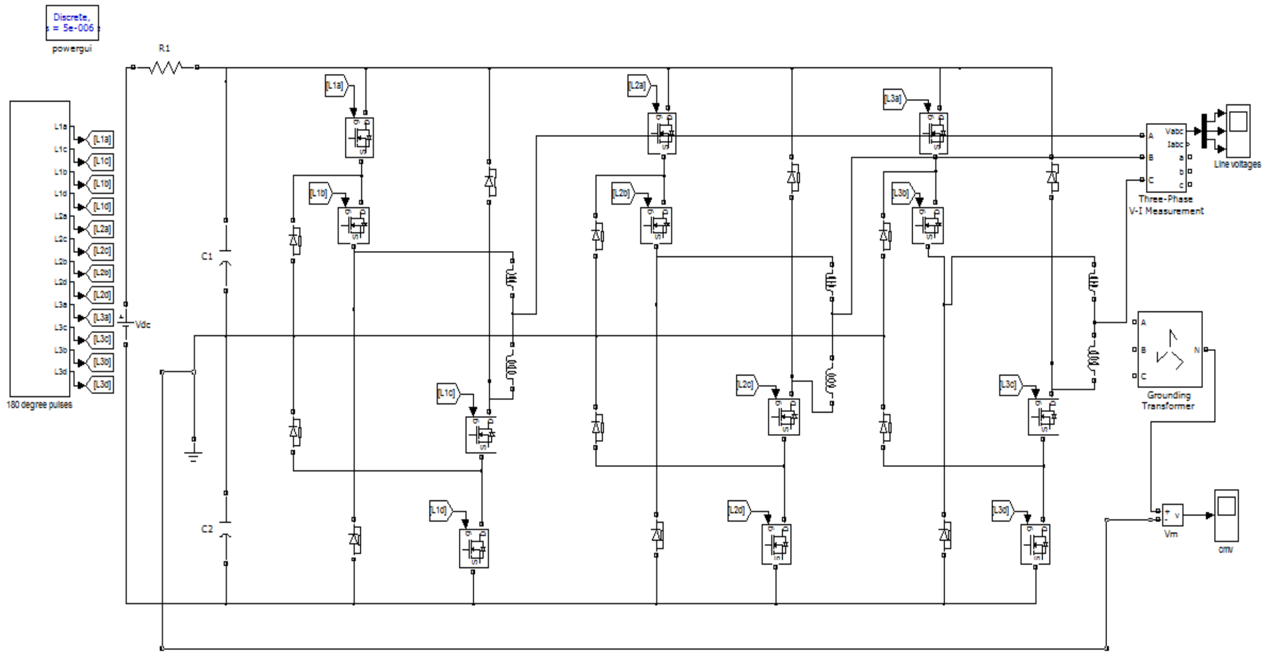

Figure.5.Simulation coupled inductor inverter (DPWM)

This is simulation of the three phase five level coupled inductor inverter. In this use only twelve switch and output get five levels. In this reduce the switches and reduce switching loss and also the reduce harmonic. This is advantage but one disadvantage inductor requires this is drawback of coupled inductor inverter.

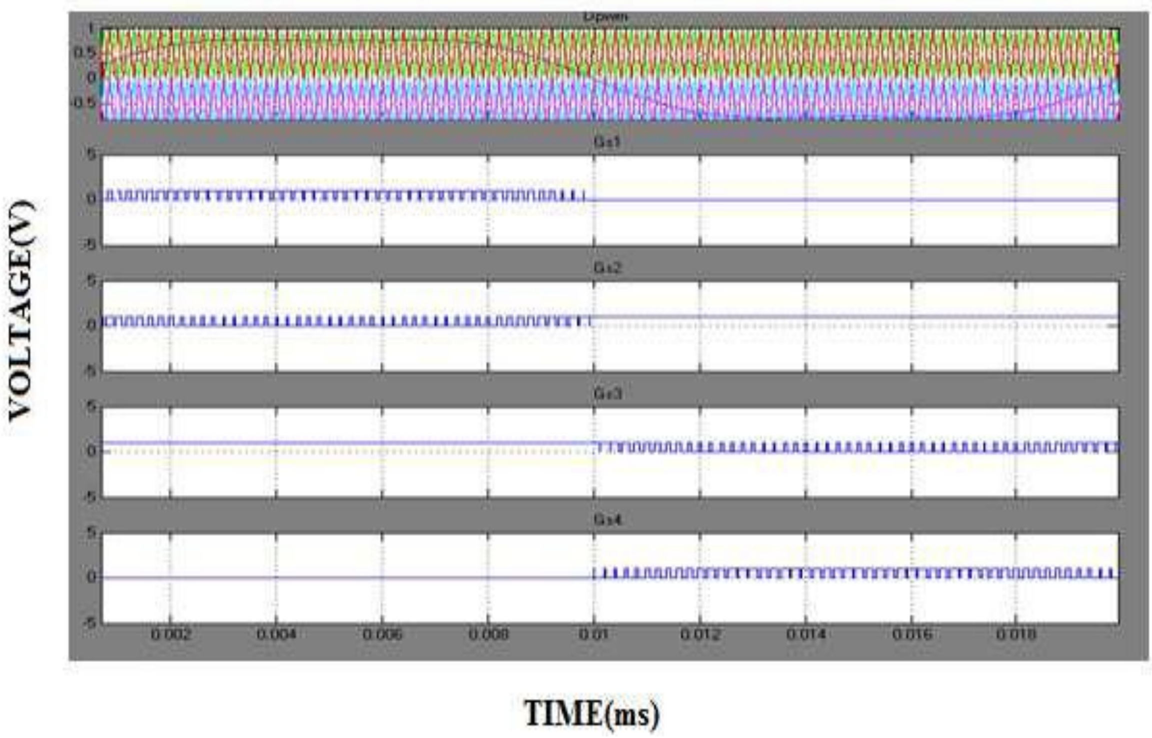

Figure.6. Discontinuous pulse modulation wave form for single phase

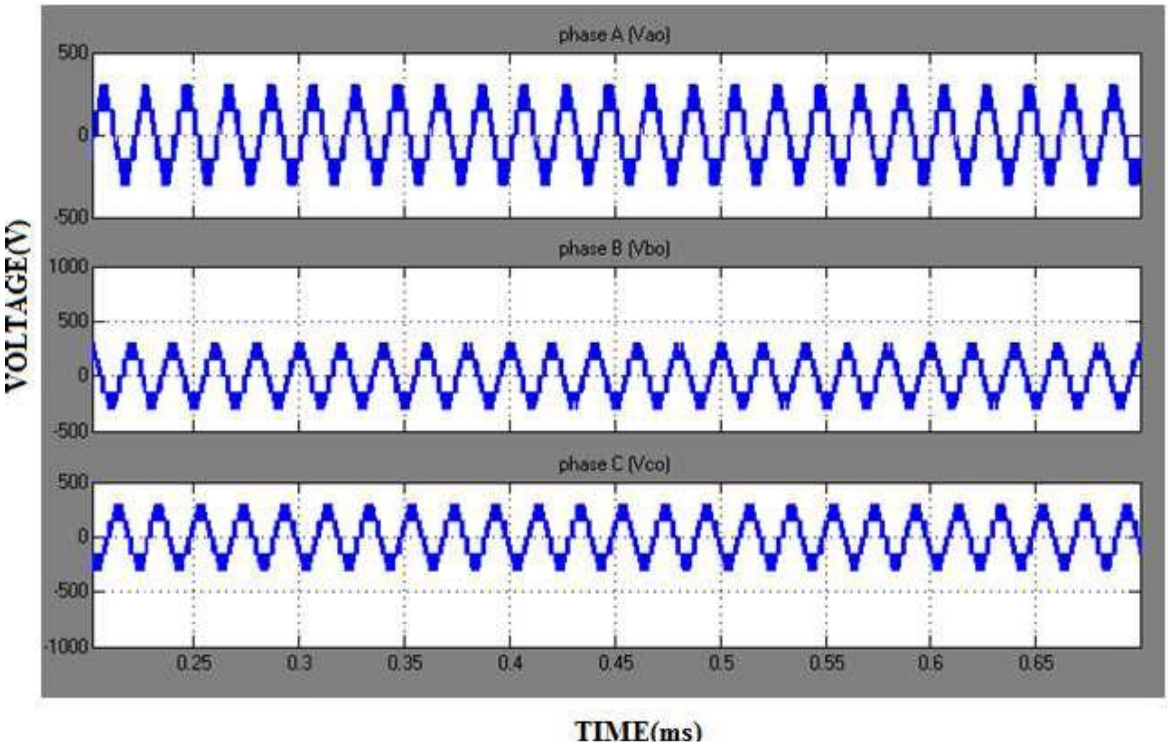

Figure.7. Wave form 3 phase 5 level coupled inductor inverter Ma=0.9, Fc=10 KHz

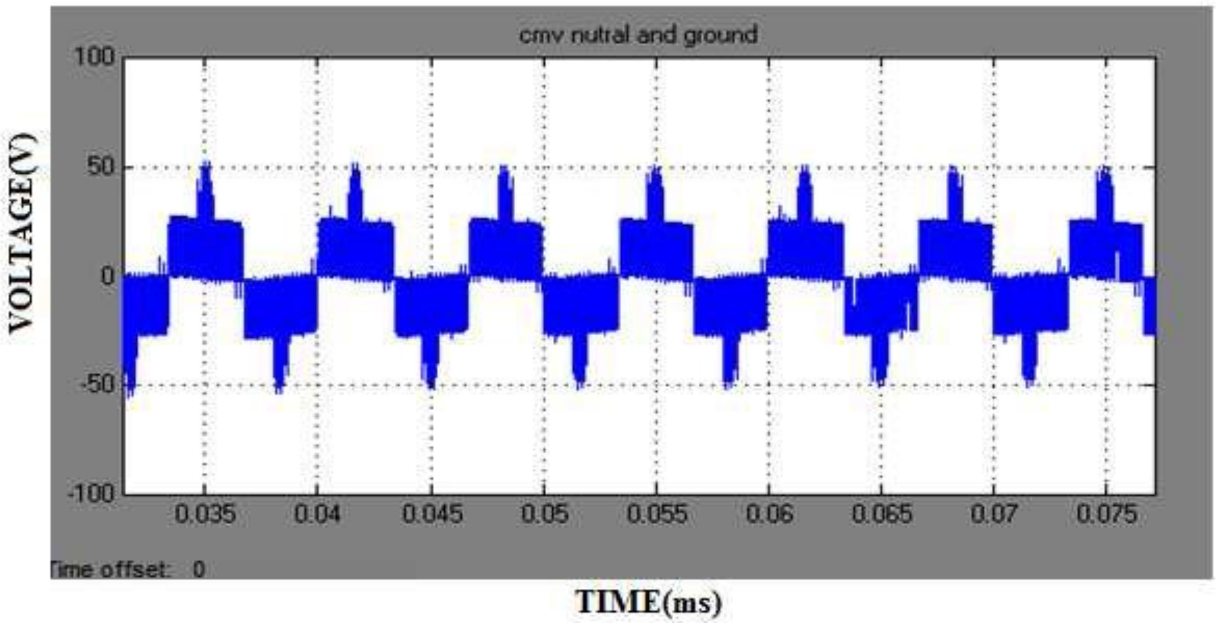

Figure.8. Wave form common mode voltage

V. CONCLUSION

A conventional continuous PWM with NPC-CII generates high CMV which is responsible for a leakage current and the premature failure of motor bearings. A multilevel inverter has the inherent ability to reduce CMV. Mathematical analysis and Simulation and results prove that the Discontinuous PWM for the NPC-CII will reduce common mode current by reducing the ripple current in the inductor. It is done by choosing the high inductance switching state due to that magnitude of CMV reduced up to Vdc/12 and it has a minimum THD in the line voltage. A multilevel inverter reduces the dv/dt in its output voltage and therefore the leakage current is also reduced.

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