



ANALYSIS OF GRID SYNCHRONIZATION TECHNIQUES FOR DISTRIBUTED GENERATION SYSTEM DURING GRID ABNORMALITIES

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Analysis of grid synchronization techniques for distributed generation system during grid abnormalities

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Abstract — This study deals with the distributed power generation system (DPGS) connected to the grid, the major issue is synchronization with grid. The phase-locked loop (PLL) is used for detecting the phase angle of the utility voltage and locking the grid phase with the incoming power source. The synchronization of power electronic converters with grid even in unbalanced and variable voltage/frequency situation is the main target of this paper. The method Synchronous Reference Frame PLL (SRF-PLL) with PI-regulator gains calculated with the symmetrical optimum method has been designed and simulations in SIMULINK have been made. Further another one method double synchronous reference frame (DSRF-PLL) has been simulated and compared both techniques. For supporting the research MATLAB simulation is utilized.

Keywords-component; SRF-PLL, PI-controller, DSRF-PLL, grid synchronization.

I. INTRODUCTION (OVERVIEW)

The use of fossil fuels for electric power generation has many problems with the environment. This, along with the day by day increasing demands of power lead to a demand of power generation using renewable energy sources, which mainly include solar power, wind power, small hydro power as a distributed generation system. [3]

These Distributed Generation (DG) systems need to be controlled properly in order to ensure sinusoidal current

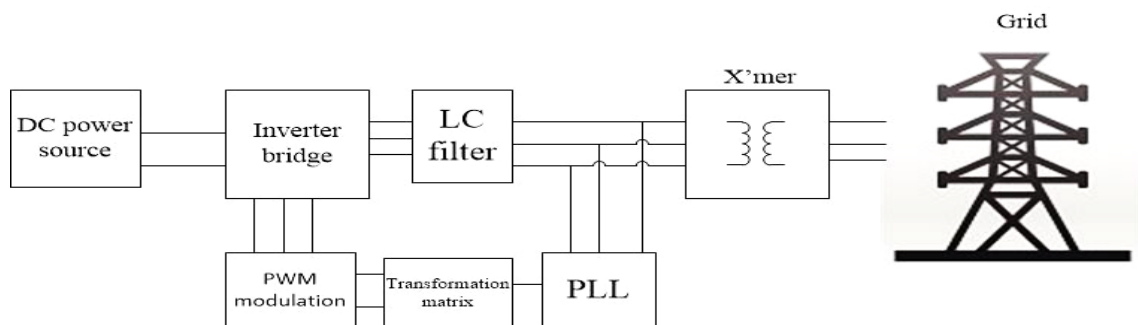


Fig. 1. Block diagram of grid connected synchronization system

injection into the grid. The major issue associated with the distributed generation system is their synchronization with utility voltage vector.

Converter of DG units must be synchronized with the utility system. Grid synchronization is a challenging task, especially when the utility signal is polluted with disturbances and harmonics or distorted frequency. The detection of the positive sequence voltage component of the fundamental frequency is required for the control of distributed generation. The magnitude and phase angle of the positive sequence voltage is used for the synchronization of the converter output variables or for the transformation of the state variables into rotating reference. The purpose of this study is to introduce the basis of the synchronization problem in grid connected systems and to present some of the most relevant structures of synchronization systems used in electric networks.

II. ANALYSIS OF THE SRF-PLL

The basic idea of the PLL system is a feedback system with a PI-regulator tracking the phase angle. Input is the three phases of the grid voltage and output from the PLL is the phase angle of one of the three phases.

There are two alternatives, either assuming the grid voltages are in balance and track only one of the phases and then shift with 120 degrees for each of the other two phases or having three PLL systems, one for each phase. [4]

In the conventional PLL, three-phase voltage vector is translated from the abc natural reference frame to the $\alpha\beta$ stationary reference frame by using Clarke's transformation, and then translated to dq rotating frame by Park's transformation as shown in Fig.2.

The angular position of this dq reference is controlled by a feedback loop which makes the d-axis component equal to zero in steady state. Therefore, under steady state condition, the q-axis component will be the voltage vector amplitude.

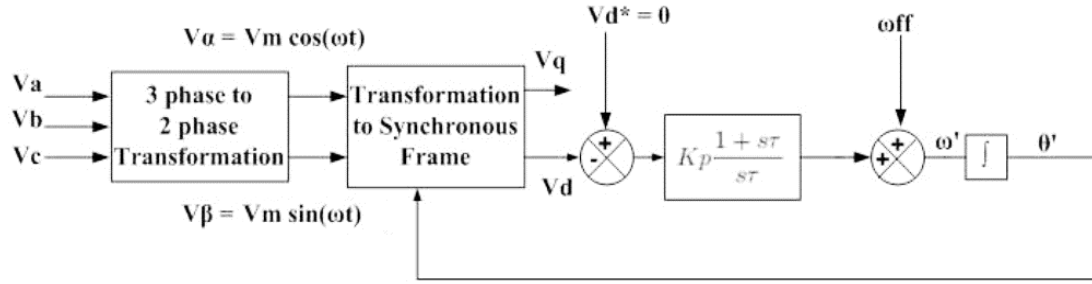


Fig. 2. Schematic diagram of SRF-PLL

2.1. Stationary reference frame αβ:

To track the phase angle the three phase voltage signals V_a , V_b and V_c are transferred from three phases to a stationary system of two phases V_α and V_β .

The grid voltages are given as:

$$V_a = V_m \sin \omega t$$

$$V_b = V_m \sin(\omega t - 2\frac{\pi}{3})$$

$$V_c = V_m \sin(\omega t + 2\frac{\pi}{3})$$

The αβ-transformation matrix by Clarke's Transformation

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

Carrying out the matrix multiplication $V_{\alpha\beta} = T_{\alpha\beta} * V_{abc}$ yields

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = V_m \begin{bmatrix} \sin(\theta) \\ \cos(\theta) \end{bmatrix}$$

which is two signals carrying information only about the phase angle of one of the phases, V_a .

2.1. Synchronous rotating reference frame:

The phase angle θ is tracked by synchronizing the voltage space vector along q or d axis in the SRF.

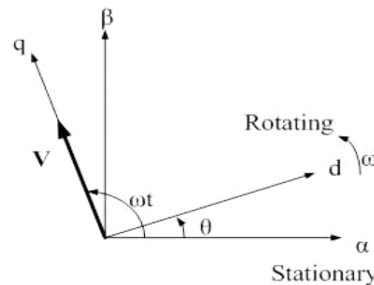


Fig. 3. Synchronous rotating reference frame.

$$\therefore \begin{bmatrix} V_q \\ V_d \end{bmatrix} = \begin{pmatrix} \sin \theta^* & \cos \theta^* \\ -\cos \theta^* & \sin \theta^* \end{pmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix}$$

$$\therefore \begin{bmatrix} V_q \\ V_d \end{bmatrix} = \begin{bmatrix} V_m \cos(\theta - \theta^*) \\ -V_m \sin(\theta - \theta^*) \end{bmatrix}$$

The estimated frequency ω' is the sum of the PI-output and the feedforward frequency ω_{ff} . Gains of the PI-regulator is then designed so that V_d follows the reference value $V_d^* = 0$. [4]

III. ANALYSIS OF THE DSRF-PLL

This method utilizes two synchronous reference frames i.e. the voltage vector v is decomposed into positive sequence phasor v^+ and negative sequence phasor v^- , as shown in Fig.

In the general equation of $V\alpha\beta$, α - and β -axis components both contain the information of the positive sequence and negative sequence which makes it difficult to detect the positive sequence component.

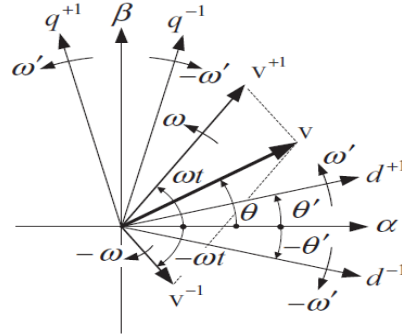


Fig. 4. Synchronous rotating reference frame.

A synthesis circuit, as shown in Fig. 5, is used to separate them. Then like two independent PLLs, the two synchronous reference frames rotating with the positive direction and negative direction respectively and detect the positive sequence and negative sequence components simultaneously.

Figure shows the positive- and negative-sequence components of the unbalanced voltage vector together with a double synchronous reference frame (DSRF) consisting of two rotating reference frames: dq^+1 , rotating with the positive speed ω' and whose angular position is θ' and dq^-1 , rotating with the negative speed $-\omega'$ and whose angular position is $-\theta'$.

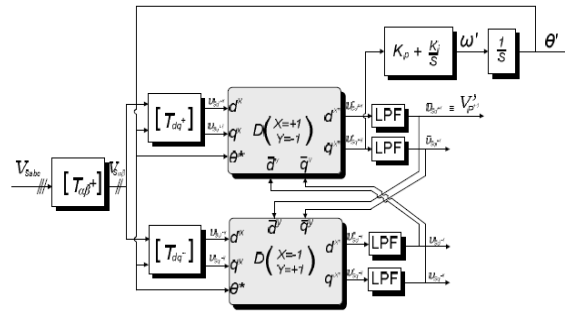


Fig. 5. Double Synchronous Reference Frame Phase Locked Loop (DSRF-PLL) (Rodriguez,2002) [1].

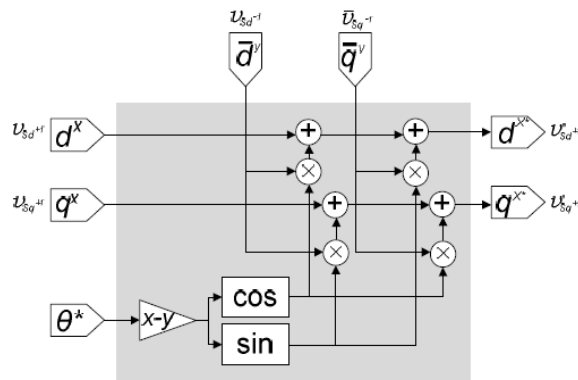


Fig. 6. Synthesis circuit for decoupling sequences (Rodriguez,2002) [1].

while the oscillations at 2ω correspond to the coupling between axes appearing as a consequence of the voltage vectors rotating in opposite directions. Therefore, instead of using any filtering technique for attenuating oscillations at 2ω , [4]

$$\begin{aligned} \mathbf{v}_{dq^{+1}} &= \begin{bmatrix} v_{d^{+1}} \\ v_{q^{+1}} \end{bmatrix} = V^{+1} \begin{bmatrix} \cos(\phi^{+1}) \\ \sin(\phi^{+1}) \end{bmatrix} + V^{-1} \begin{bmatrix} \cos(2\omega t) & \sin(2\omega t) \\ -\sin(2\omega t) & \cos(2\omega t) \end{bmatrix} \begin{bmatrix} \cos(\phi^{-1}) \\ \sin(\phi^{-1}) \end{bmatrix} \\ \mathbf{v}_{dq^{-1}} &= \begin{bmatrix} v_{d^{-1}} \\ v_{q^{-1}} \end{bmatrix} = V^{-1} \begin{bmatrix} \cos(\phi^{-1}) \\ \sin(\phi^{-1}) \end{bmatrix} + V^{+1} \begin{bmatrix} \cos(2\omega t) & -\sin(2\omega t) \\ \sin(2\omega t) & \cos(2\omega t) \end{bmatrix} \begin{bmatrix} \cos(\phi^{+1}) \\ \sin(\phi^{+1}) \end{bmatrix} \end{aligned}$$

These expressions clearly give evidence that the AC terms in the dq+1 axes result from the DC terms in the dq-1 axes being affected by a rotating transformation matrix at 2ω frequency.

A similar conclusion can be obtained for AC signals on the dq-1 reference frame. [6]

LPF block is a low-pass filter such as:

$$LPF(s) = \frac{\omega_f}{s + \omega_f}$$

Where ω_f = Cut off frequency of low pass filter. [4]

IV. PERFORMANCE COMPARISON OF THE THREE-PHASE PLL ALGORITHMS:

System characteristics for SRF-PLL:

The grid voltage level is 1kV. This value is the root mean square value of the line-to-line voltage. The amplitude voltage level, V_m , is then calculated according to

$$V_m = \sqrt{\frac{2}{3}} \cdot 1000 = 816V$$

The frequency of the utility grid is 50Hz.

sampling time is set to $T_s = 10\text{e-}6$ sec.

PI components: $k_i = 1.0132$, $K_p = 0.3848$. calculated using Symmetrical optimum (SO) method. [7]

SIMULINK is powerful tool for control and signal processing simulations. With the help of MATLAB R2013a

Simulation parameters:

- Simulation time is set from 0.0 to 3s
- Solver is set to Discrete (no continuous states)
- Type is set to Fixed step
- Sampling time is set to $= 10\text{e-}6\text{s}$.

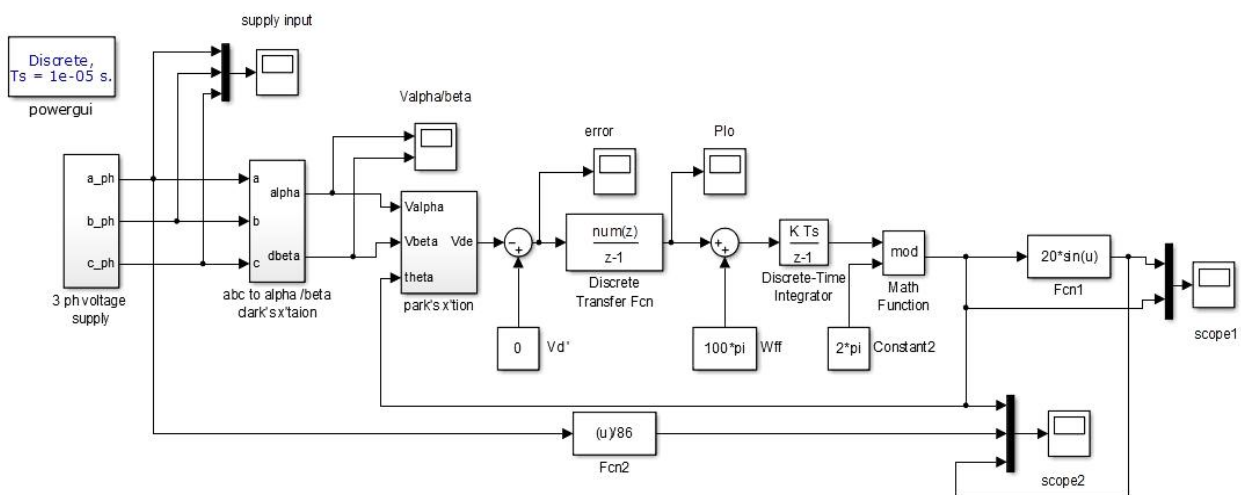


Fig. 7. The Simulink simulation setup of the SRF- PLL system.

4.1 Simulation for ideal grid conditions:

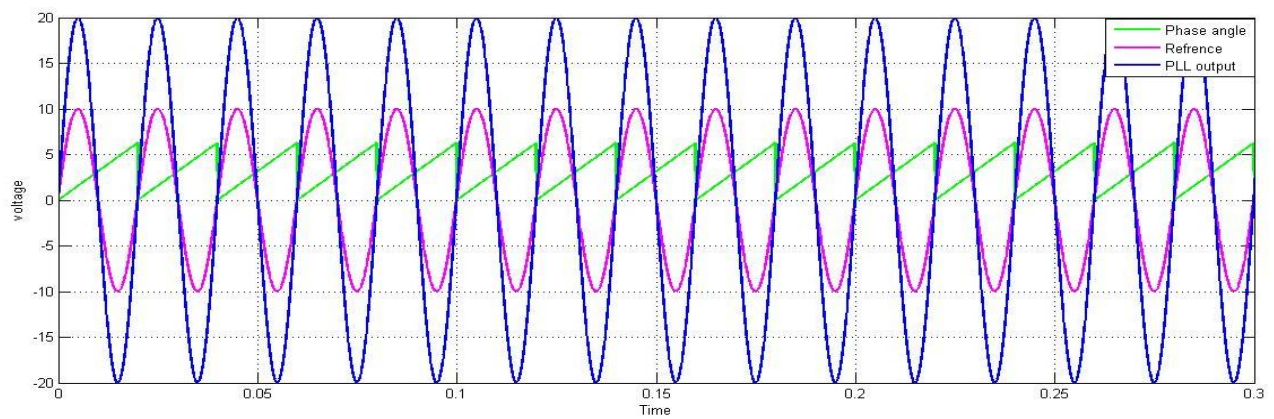


Fig. 8. PLL output with ideal grid conditions.

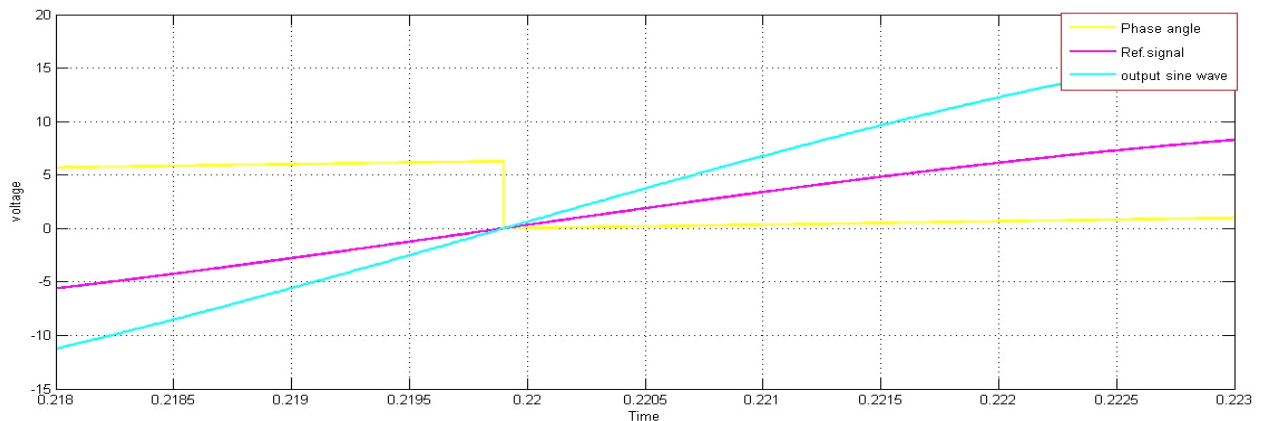


Fig. 9. PLL output with ideal grid conditions. (zoomed)

4.2 Simulation results during Abnormalities:

Amplitude variation:

The amplitude is varied in a way that after 1 sec the amplitude decreases to 70% of the original value see figure below.

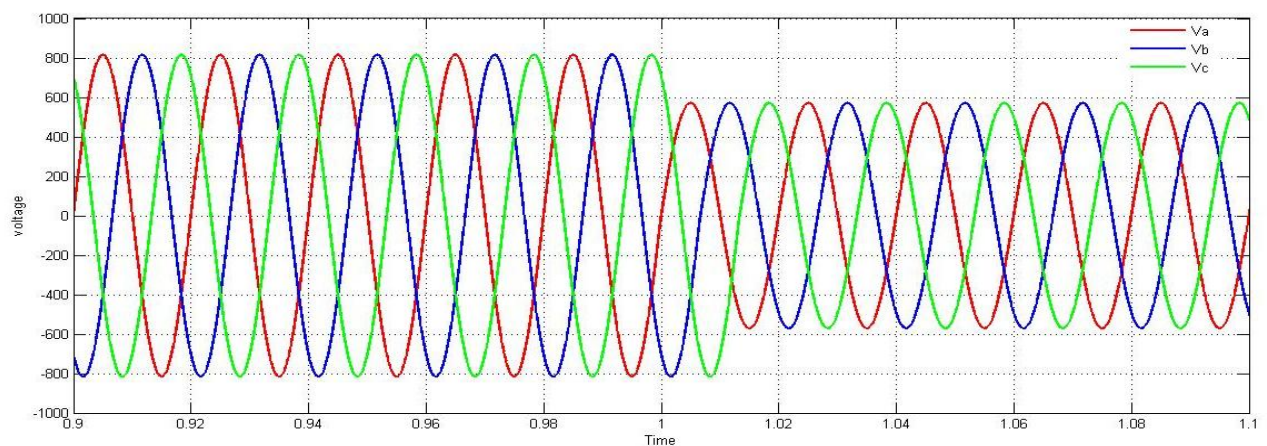


Fig. 10. Input signals with amplitude decreasing to 70% of the original value.

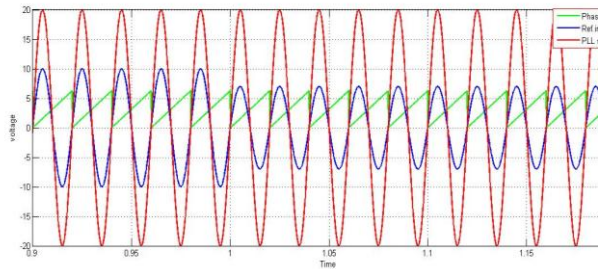


Fig. 11. PLL output for input with decreased amplitude.

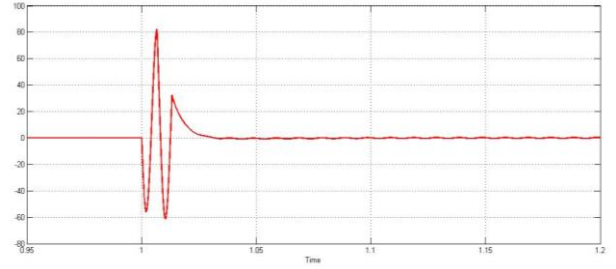


Fig. 12. output of scope 2 for error signal

Three phase voltage unbalance: input signal
 $V_a=816V, V_b=835V$ & $V_c=797V$.

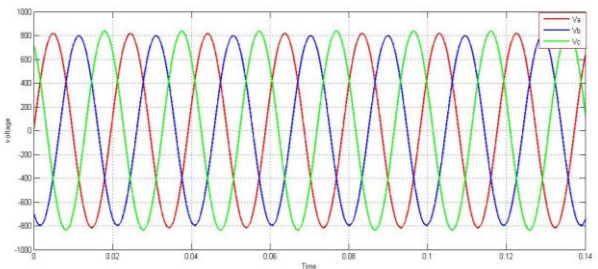


Fig. 13. input signal with unbalanced input signal

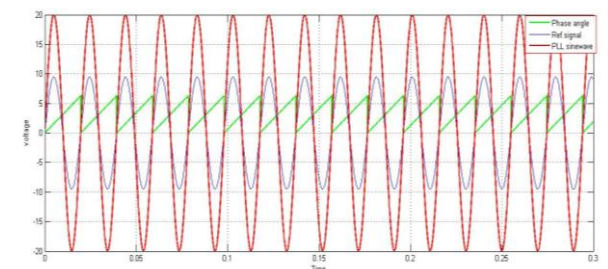


Fig. 14. PLL output with input unbalanced signals.

4.3 System characteristics for DSRF-PLL:

Amplitude variation:

All input parameter would be same except PI constants.
simulations. With the help of MATLAB R2013a

Simulation parameters:

- Simulation time is set from 0.0 to 3s
- Solver is set to Discrete (no continuous states)
- Type is set to Fixed step
- Sampling time is set to = 10e-6s
 $k_i = 0.531, K_p = 1.731e-8$.

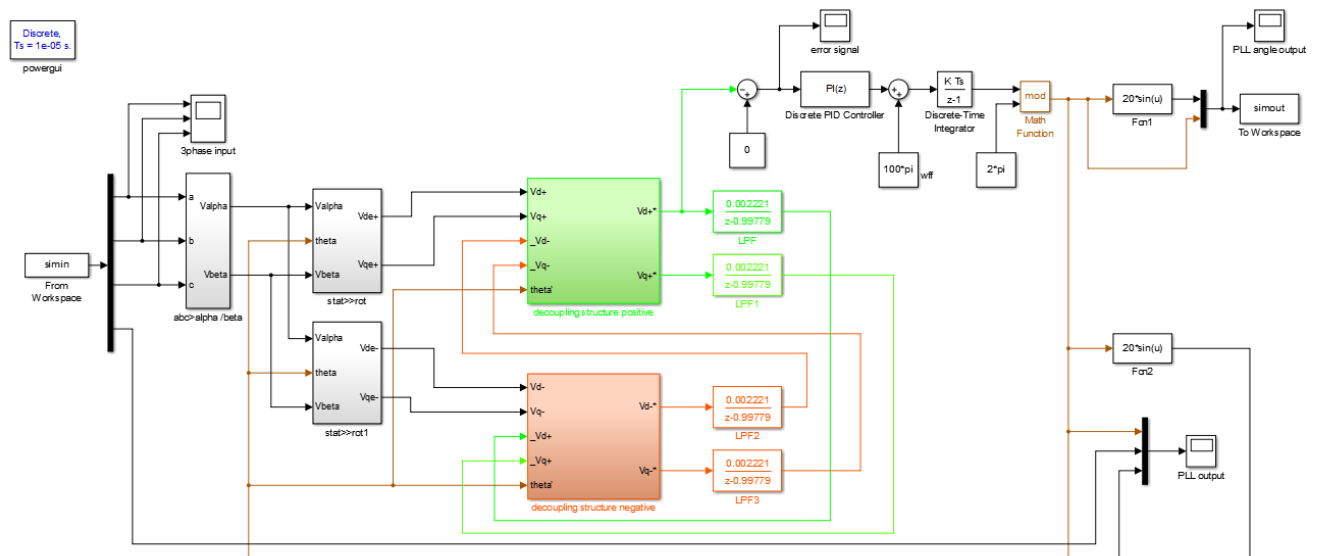


Fig. 15. Simulink model of Double Synchronous Reference Frame Phase Locked Loop (DSRF-PLL)

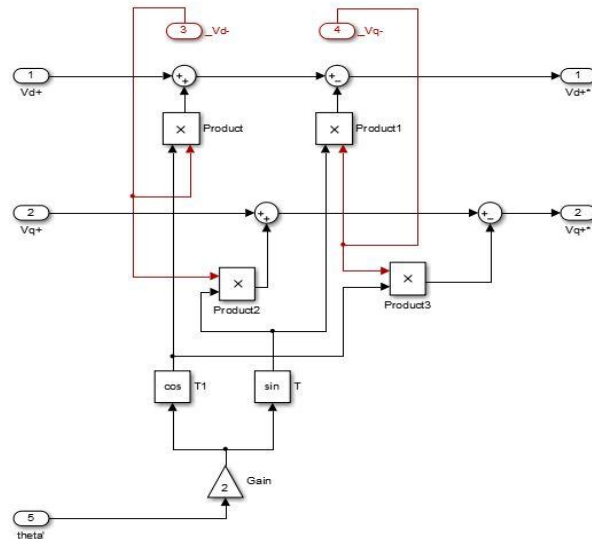


Fig. 16. Synthesis circuit for decoupling sequences Simulation result during ideal case:

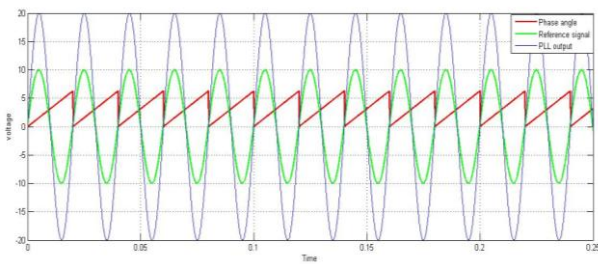


Fig. 17. Synchronized PLL signals in DSRF-PLL

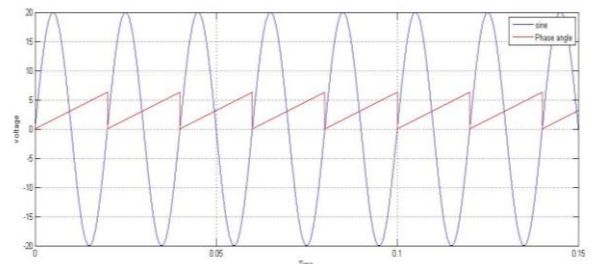


Fig. 18. Phase detection using DSRF simulation

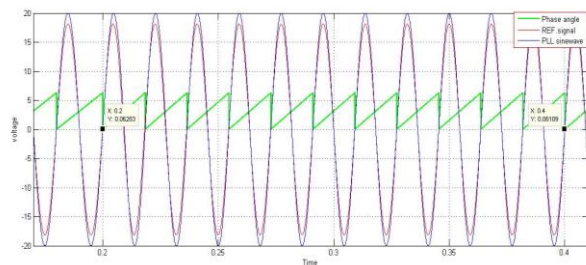


Fig. 19. PLL output of frequency step change from 50Hz to 55 Hz.

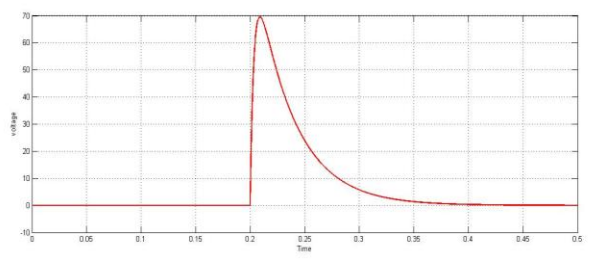


Fig. 20. output scope results for error signal. Here by DSRF-PLL results settling time noticed of 0.2sec.

V.CONCLUSION

A PLL system has been designed and tested with simulations in SIMULINK. The PI-regulator gains $K_p=0.3848$ and $k_i=1.0132$ were calculated with the SO method. For ideal grid conditions, with amplitude $V_m = 816V$ and frequency $f = 50Hz$, the phase angle was tracked fast and accurate.

The system was simulated for several non-ideal grid conditions. Variations in amplitude and frequency were handled well by the system.

Also implemented DSRF-PLL method on MATLAB simulation still got the proper synchronization during ideal condition.

Acknowledgment

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