



Vedic Multiplier Using Efficient Compressor to Reduce the Delay for Vedic Multiplier and Pipelining

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Abstract — With the new technology and new innovation in the VLSI, it is used for the high speed communication and the signal processing. Vedic mathematics gives the fast operation and it reduces the delay and almost power constant. So we can perform the fast operation and can calculate fastly with the help of Vedic mathematics. The structure uses 15:2 compressor using 3:2 and 7:2 compressor architecture. In addition it uses “Urdhwa Tiryakbhyam Sutra” of Vedic mathematics and reducing the delay using pipelining technique. This all procedure is carried out in Xilinx ISE Design Suite 13.2_1 software and gives us the delay and power get improve. More often than not, performance of microcontrollers and Digital signal processors are evaluated on the basis of number of multiplications performed in unit time. Hence better multiplier architectures are bound to increase the efficiency of the system. Vedic multiplier is one such promising solution. Its simple architecture coupled with increased speed forms an unparalleled combination for serving any complex multiplication computations. Vedic multiplier known as “Urdhwa Tiryakbhyam” meaning vertical and crosswise implemented using reversible logic, which is the first of its kind. This multiplier may find applications in Fast Fourier Transforms (FFTs), and other applications of DSP like imaging, software defined radios, wireless communications.

Keywords- High Speed Multiplier, 3:2 Compressors, 15:2 Compressor, Urdhwa Tiryakbhyam, Vedic Multiplier.

I. INTRODUCTION

The processor speed greatly depends on its multiplier's performance. This in turn raises the demand for multipliers high speed, at the same time maintaining low area and moderate power dissipation. Over the past few decades, several new novel architectures are come for multipliers and have been designed and explored. Booth's and modified Booth's algorithm based multipliers are quite popular in modern VLSI design but come along with their own set of disadvantages. In these multiplier algorithms, the multiplication process, involves several transitional operations before received at the finishing answer. The intermediate stages include several additions, subtractions and comparisons which reduce the speed exponentially with the total number of bits present in the multiplier and the multiplicand. Since the speed is major concern, utilizing such type of architectures is not good approach since it involves several time consuming operations. In order to address the disadvantages of the above mentioned methods with respect to speed of operation, explored a new approach for multiplier design based on ancient vedic mathematics. Vedic mathematics is an Indian ancient and eminent approach which acts as a foundation to solve many mathematical challenges faced in the current day scenario. Vedic mathematics was existed in ancient India and rediscovered by a popular great mathematician, Sri Bharati Krishna Tirthaji. He divided the Vedic mathematics into 16 simple sutras (formulae). These Sutras deals with Arithmetic, Analytical, Algebra, Geometry, Trigonometry, etc. The simplicity in the Vedic mathematics sutras pays a way for its application in several prominent domains of engineering and technology like Signal Processing, Control Engineering and VLSI. One of the highlights in Vedic mathematics approach is that the calculation of all partial products required for multiplication, are obtained well in development, much before that the actual operations of multiplication begin. These intermediate partial products are then added based on the Vedic mathematics algorithm to obtain the ending product. This in turn indications to a very high speed approach to achieve multiplication. A novel method to further enhance in speed of a Vedic multiplier by replacing the existing full adders and half adders of the Vedic mathematics based multipliers with compressors based adders. Compressors, in its several variants, are logic circuits which are skilled of adding more than 3 bits at a time as divergent to a full adder and capable of acting with a lesser gate count and higher speed in comparison with an equivalent full adder circuit.

Firstly Urdhwa tiryakbhyam sutra is implemented to digital system by coding it in VHDL and then it is synthesized in quartus II. The architecture obtained from quartus II is almost similar to the architecture of array multiplier and the number of multiplications are also same. This algorithm also determines the effectiveness to reduce the $N \times N$ multiplier design module into a 4×4 multiplier design modules. Then we discussed Nikhilam Sutra which is more efficient for multiplication of bigger number. Since it reduces the complex multiplications into a simple one. The proposed Vedic multiplication is demonstrated to show its effective delay, efficiency and hierarchy design by consider an example of

4×4-bit multiplication and then it is reduced to the operation of a single 2×2-bit multiplication. The Multiplier is implemented based on the Urdhva tiryakbhyam sutra which is one of the sutras of ancient India Vedic mathematics which means vertically and crosswise algorithm. The Vedic multiplier is implemented based on the one of the sutras that is mentioned in the above list. These sutras have been usually used in the decimal number system for the product of two numbers. In this thesis, the similar idea is applied to the binary system in an appropriate way using the digital hardware of the suggested algorithm. Vedic multiplication based on some algorithms such as urdhva tiryakbhyam.

Multiplication is one of the fundamental blocks in almost all the arithmetic logic units. This Vedic multiplication is mainly used in the fields of the Digital Signal Processing (DSP) and also in so many applications like Fast Fourier Transform, convolution, filtering and microprocessor applications. In most of the DSP algorithms multiplier is one of the key component and hence a high speed and area efficient multiplier is needed and multiplication time is also one of the predominant factor for DSP algorithms. The ancient mathematical techniques like Vedic mathematics used to reduce the computational time such that it can increase speed and also requires less hardware. There are sixteen sutras and sixteen sutras (sub formulae) constructed by swahiji. Vedic is a word obtained from the word “Veda” and its meaning is “store house of all knowledge”. Vedic mathematics mainly consists of the 16 sutras which it can be related to the different branches of mathematics like algebra, arithmetic geometry.

1. Anurupye Shunyamanyat – If one is in ratio, the other is zero.
2. Chalana- Kalanabyham – Differences and Similarities.
3. Ekadhik in a Purvena – By one more than the previous One.
4. Ekanyunena Purvena – By one less than the previous one.
5. Gunaka samuchyah – The factors of the sum is equal to the sum of the factors.
6. Gunita Samuchyah – The product of the sum is equal to the sum of the product.
7. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
8. Paraavartya Yojayet – Transpose and adjust.
9. Purana Purana Byham – By the completion or non completion.
10. Sankalana- vyavakalanabhyam – By addition and by subtraction.
11. Shesha Yankena Charamena – The remainders by the last digit.
12. Shunyam Saameya Samuccaye – When the sum is the same that sum is zero.
13. Sopanty Advayamantyam – The ultimate and twice the penultimate.
14. Urdhwa-Tiryakbhyam – Vertically and crosswise.
15. Vyashtisamanstih – Part and Whole.
16. Yaavadunam – Whatever the extent of its Deficiency.

These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century.

II. LITERATURE REVIEW

Honey Durga Tiwari, Ganzorig Gankhuyag, Chan Mo Kim, Yong Beom Cho [1] introduced vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). The algorithms based on conventional mathematics can be simplified and even optimized by the use of Vedic Sutras. These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), this paper introduced new multiplier and square architecture is proposed based on algorithm of ancient Indian Vedic Mathematics, for low power and high speed applications. It is based on generating all partial products and their sums in one step. The design implementation on ALTERA Cyclone –II. A multiplier architecture based on this Sutra has been developed and is seen to be similar to the popular array multiplier where an array of adders is required to arrive at the final product. Due to its structure, it suffers from a high carry propagation delay in case of multiplication of large numbers. [1]

The M. Ramalatha, Deena Dayalan, P. Dharani, Deborah Priya, introduced reduce the load by supplementing the main processor with Co-Processors, which are designed to work upon specific type of functions like numeric computation, Signal Processing, Graphics etc. The ever increasing demand in enhancing the ability of processors to handle the complex and challenging processes has resulted in the integration of a number of processor cores into one chip. Still the load on the processor is not less in generic system. The speed of ALU depends greatly on the multiplier. In algorithmic and structural levels, numerous multiplication techniques have been developed to enhance the efficiency of the multiplier which concentrates in reducing the partial products and the methods of their addition but the principle behind multiplication remains the same in all cases.

Though there are many sutras employed to handle different sets of numeric, exploring each one gives new results. Our work has proved the efficiency of Urdhwa Triyakbhyam– Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of intermediate products, eliminates unwanted multiplication steps with zeros and scaled to higher bit levels using Karatsutra algorithm with the compatibility to different data types. This sutra is to be used to build a high speed power efficient multiplier in the coprocessor. [2]

L. Sriraman, T. N. Prabakar proposed multiplier can multiply two variables. A novel multiplier architecture based on ROM approach using Vedic Mathematics is proposed. This multiplier's architecture is similar to that of a Constant Co efficient Multiplier (KCM). However, for KCM one input is to be fixed. The proposed multiplier is implemented on a Cyclone III FPGA, compared with Array Multiplier and Urdhava Multiplier for both 8 bit and 16 bit cases and the results are presented. The proposed multiplier is 1.5 times faster than the other multipliers for 16x16 case and consumes only 76% area for 8x8 multiplier and 42%area for16x16 multiplier. In the proposed multiplier for higher order bit multiplication i.e. for 16x16 and more, the multiplier is realized by instantiating the lower order bit multipliers like 8x8.This is mainly due to memory constraints. Effective memory implementation and deployment of memory compression algorithms can yield even better results. [3]

III. PROPOSED WORK

3.1 Design of 8 Bit Vedic Multiplier Using Compressor

Algorithms for 8 X 8 Bit Multiplication Using Urdhva Tiryakbhyam (Vertically and crosswise) for two Binary numbers

Consider 8X8 bit binary number as A and B. So, bit multiplication will be as follows.

A = A7A6A5A4A3A2A1A0

B = B7B6B5B4B3B2B1B0

Make the partition into equal part of A and B.

AH = A7A6A5A4,

AL = A3A2A1A0.

BH = B7B6B5B4,

BL = B3B2B1B0.

Finally, according to Urdhava Tiryakbhyam Sutra,

$A \times B = AL \times BL + AH \times BL + AL \times BH + AH \times BH$

The final equation shows the result multiplication using Vedic Sutra. The process is followed according to the steps shown in Figure4.4

Block Diagram:

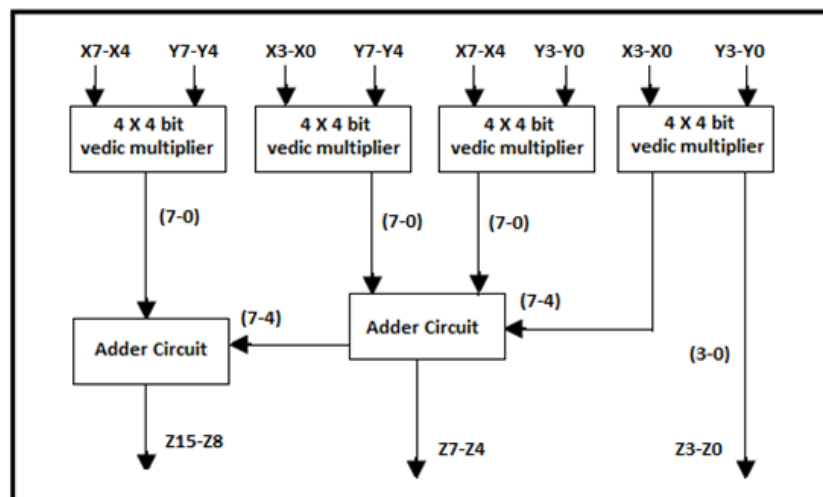


Figure 1: Hardware realization of 8x8 bit multiplication using UrdhwaTiryakbhyam Sutra.

3.2 STEP TO DESIGN 8X8 BIT VEDIC MULTIPLIER

- 3.2.1 One bit Full Adder
- 3.2.2 Eight bit Full Adder
- 3.2.3 4X4 Bit Vedic Multiplier
- 3.2.4 8X8 Bit Vedic Multiplier

3.2.1 One Bit Full Adders

Circuit Diagram

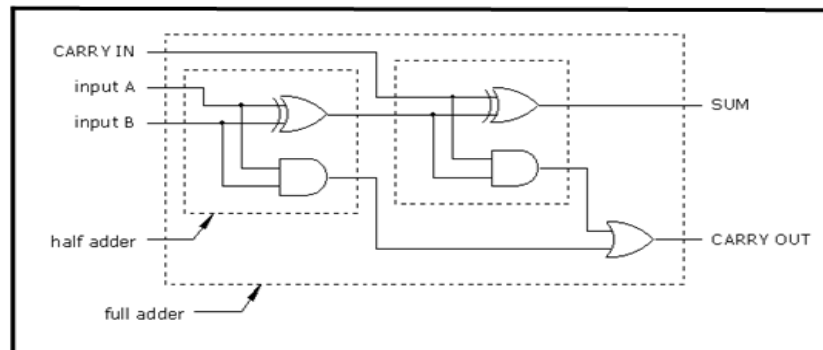


Figure 2: One Bit Full Adder

Working

A full adder is a combinational circuit that performs the arithmetic sum of three bits: A, B and a carry in, C, from a previous addition. One way of implementing a full adder is to utilize two half adders in its implementation. The full adder is the basic unit of addition employed in all the adders. The sum of A and B are fed to a second half adder, which then adds it to the carry in C (from a previous addition operation) to generate the final sum S. The carry out, Co, is the result of an OR operation taken from the carry outs of both half adders. There are a variety of adders in the literature both at the gate level and transistor level each giving different performances.

Boolean Equations:

$$S = C \oplus (A \oplus B)$$

$$Co = AB + C(A \oplus B)$$

3.2.2 Eight Bit Full Adder

Circuit diagram

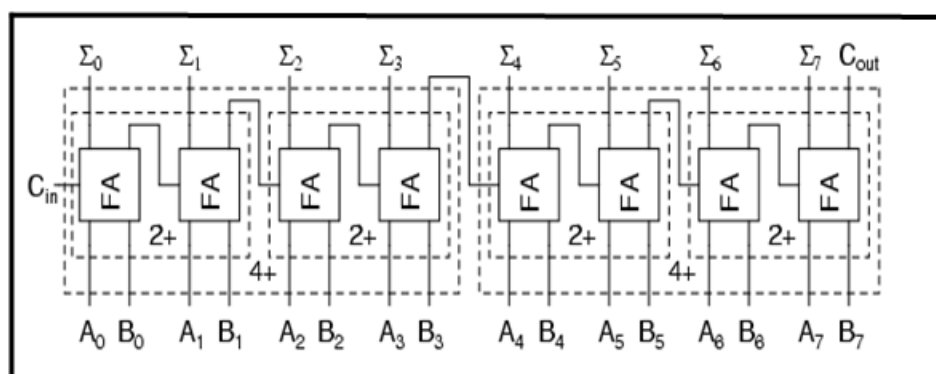


Figure 3: Eight Bit Full Adder

Working

The figure above is an eight bit full adder. The two 2-bit adders to make a 4-bit adder and then using two 4-bit adders to make an 8-bit adder. Each "2+" is a 2-bit adder and made of two full adders. Each "4+" is a 4-bit adder and made of two 2-bit adders. And the result of two 4-bit adders is the same 8-bit adder we used full adders to build.

For any large combinational circuit there are generally two approaches to design you can take simpler circuits and replicate them; or you can design the complex circuit as a complete device. Using simpler circuits to build complex circuits allows us to spend less time designing but then requires more time for signals to propagate through the transistors. The 8-bit adder design above has to wait for all the C_{out} signals to move from $A_0 + B_0$ up to the inputs of Σ_7

Boolean equation:

$$SUM = A_i \oplus B_i \oplus C_i$$

$$C_{out} = C_i + 1 = A_i B_i + (A_i \oplus B_i) C_i$$

3.2.3 Design of 4X4 Bit Multiplier

Let's analyze 4x4 multiplications, say $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$. Following are the output line for the multiplication result, $S_7S_6S_5S_4S_3S_2S_1S_0$. Let's divide A and B into two parts, say A_3A_2 & A_1A_0 for A and B_3B_2 & B_1B_0 for B. Using the fundamental of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block, we can have the following structure for multiplication.

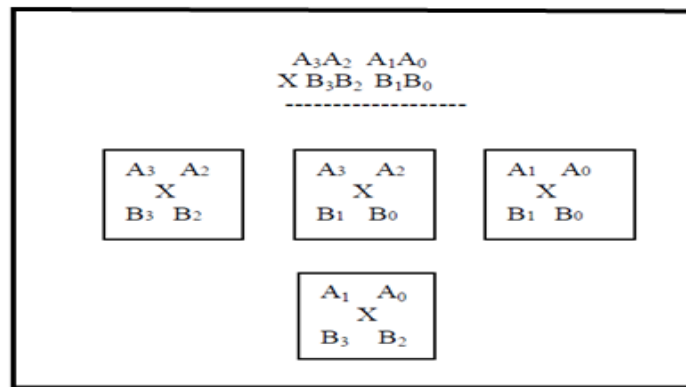


Figure 4: Algorithm for 4 bit Vedic Urdhwa Multiplier

BLOCK DIAGRAM

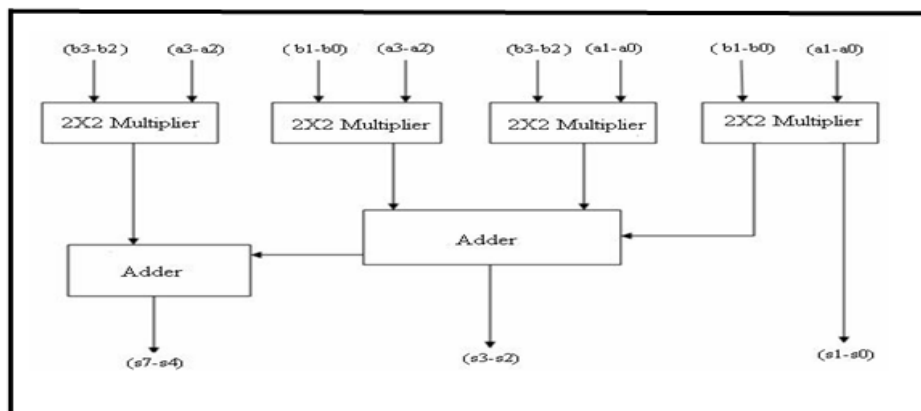


Figure 5: 4x4 bit Multiplier

Working

To design 4X4 multiplier we need to design 2X2 multiplier and carry save adder. With the help of 2X2 multiplier and ripple carry adder. We finally get the circuit of 4x4 bit Vedic multiplier by using shift add method. In shift add method we keep initial carry zero and sequentially adding is done. The function of each block of 4X4 Vedic multiplier is as given below:

2X2 Multiplier

Diagram

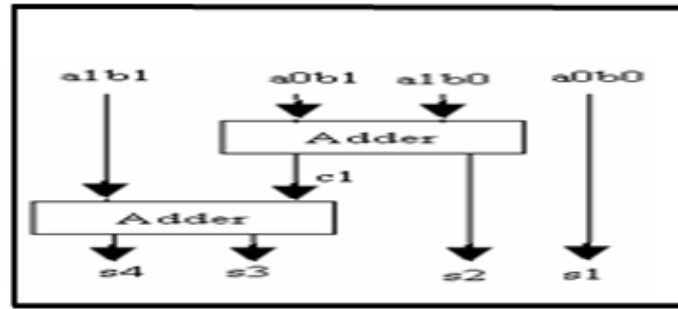


Figure 6 : Multiplication of 2X2 bit using Urdhwa Tiryakbhyam Sutra Working

For Multiplier, first the basic blocks that are the 2x2 bit multipliers have been made and then, using these blocks, 4x4 blocks has been made by adding the partial products using adder circuits and then using this 4x4 block the 8x8 bit multiplier block is implemented. The 8 bit input A and B are given to the 4X4 Vedic multiplier block which generate the output to be manipulate into adder circuit to obtained the output given.

4 bit Ripple Carry Adder

Circuit diagram

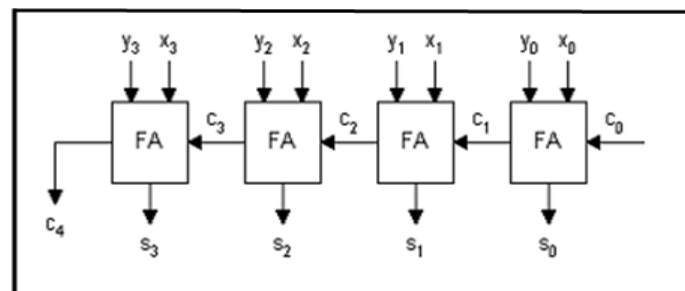


Figure 7: 4 bit Ripple Carry Adder

Working

In the ripple carry adder, the output is known after the carry generated by the previous stage is produced. Thus, the sum of the most significant bit is only available after the carry signal has rippled through the adder from the least significant stage to the most significant stage. As a result, the final sum and carry bits will be valid after a considerable delay.

3.2.4 Design 8X8 Bit Vedic Multiplier

Block diagram

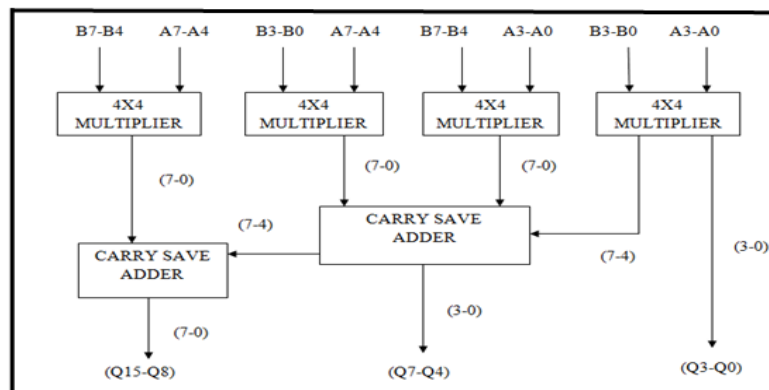


Figure 8: 8X8 Bit Vedic Multiplier using Urdhwa T. Method Working

The 8 x 8 bit multiplier is structured using 4X4 bit blocks as shown in figure 4.11. In this figure the 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The 16 bit product can be written as:

$$P = A \times B = (AH-AL) \times (BH-BL)$$

$$= AH \times BH + AH \times BL + AL \times BH + AL \times BL$$

The outputs of 4X4 bit multipliers are added accordingly to obtain the final product. Thus, in the final stage two carry save adders are also required. Previously we design the 4 bit carry save adder in the 4X4 bit multiplier. In the same way here also we use two 8 bit adder.

Now the basic building block of 8x8 bits Vedic multiplier is 4x4 bits multiplier which implemented in its structural model. For bigger multiplier implementation like 8x8 bits multiplier the 4x4 bits multiplier units has been used as components which are implemented already in ModelSim6.1e or Xilinx ISE9.1i library. The structural modeling of any design shows fastest design.

RESULT = (Q15- Q8) & (Q7- Q4) & (Q3-Q0)

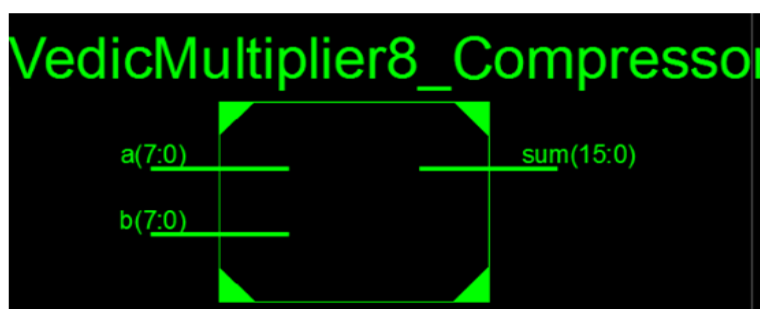


Figure 9: Block representation of 8x8 Vedic multiplier

3.3 Pipelining Structure

Pipelining is an important technique used to speed up the clock frequency in all Digital signal processors and current generation processors. The beauty of pipelining design is that new data is being processed before the processing of the prior data has finished. The performance of the proposed multiplier is advanced by the implementation of pipelined concept.

The execution performance is improved with pipeline when compared with sequential traditional execution. In a pipeline a task is divided into subtask and subtasks are executed simultaneously. In Vedic multiplier the multiplier and multiplicand are subdivided and applied at individual stages of pipeline. The parallel multiplier such as Vedic multiplier effectively solves a 4bit or 8bit multiplication on 8-bit processor. Sometimes lower word length microprocessor alone cannot compute higher bit multiplication. For large scale computation pipeline is the best solution to perform faster operation.

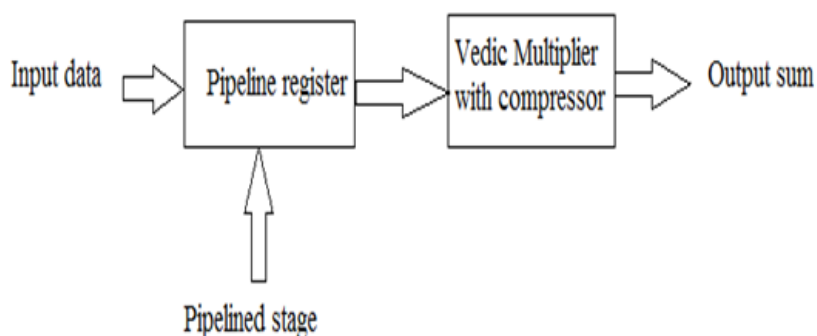


Figure 10: Basic block diagram of Vedic multiplier using pipeline technique

IV. SIMULATION RESULTS

4.1 Result Comparison with Normal Vedic Multipliers

To perform the comparison in between various multipliers such as Urdhwa Tiryakbhyam, compressor based Urdhwa Tiryakbhyam, modified compressor based Urdhwa Tiryakbhyam multiplier and compressor based Urdhwa Tiryakbhyam using pipelining technique were designed implemented on Xilinx ISE Design Suite 13.2_1 Spartan 6 family for reducing the delay and improve power.

Table1: Comparison of Normal Vedic Multiplier and Compressor Based Vedic Multiplier Architectures

For Delay

Type	Normal Vedic Multiplier	Vedic Multiplier with Compressor	% Improvement
8*8	13.75 ns	5.60 ns	59.36 %

For Power

Type	Normal Vedic Multiplier	Vedic Multiplier with Compressor	% Improvement
8*8	13.55 mw	10 uw	75.01 %

It can be clearly noted from Table I., that in terms of speed, the compressor based Vedic maths multiplier performs exceptionally well and faster than the existing Vedic maths based multiplier.

Table 2 : Analysis result of LUT's, power and delay

Algorithm Used	LUT's Used	Power (W)	Delay(nsec)
Compressor based Urdhwa Tiryakbhyam	170	13.55m	20.16
Modified Compressor based Urdhwa Tiryakbhyam Multiplier	126	13.55m	13.78
Compressor based Urdhwa Tiryakbhyam Multiplier using Pipelining	86	10u	5.60

From the synthesis report it is clear that the area utilization and total delay of the vedic multiplier with pipelining stage is improved.

4.2 Graph of Different 8*8 Bit Multipliers

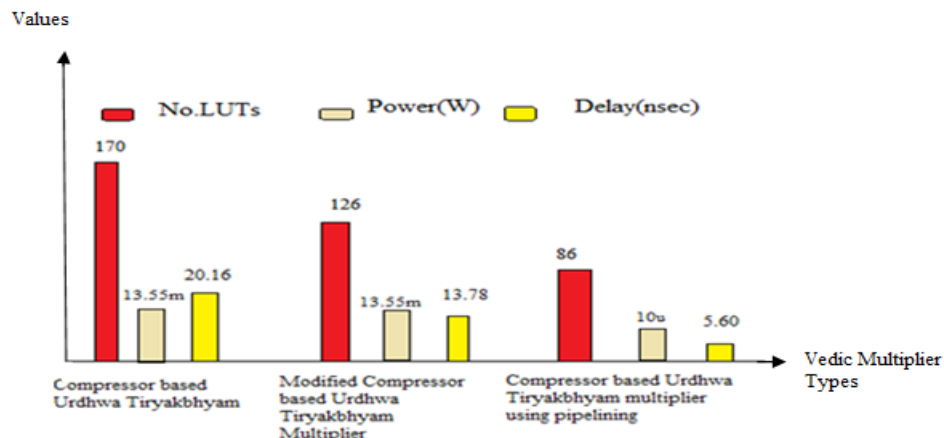


Figure 11: Graph of different 8*8 bit multipliers

The graph shows the comparison between the various based multiplier. It is observe that the compressor based Urdhwa Tiryakbhyam multiplier using pipelining structure the delay is reduced and power get improved as compared to the other multiplier used in earlier. The multiplication of two 8 bit binary number i.e. a=01110111 and b=01110011 the output result is 001101011110101. following figure shows the output waveform using Xilinx ISE Design Suite 13.2_1.

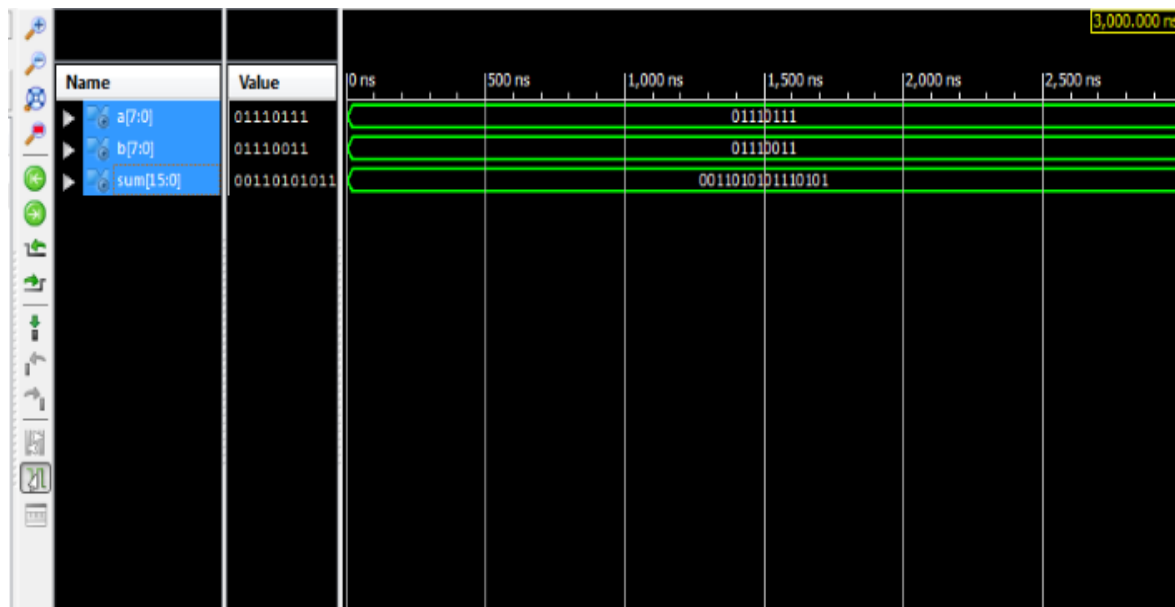


Figure 12: 8×8 bit multiplication using compressor based multiplier

Following figure shows the timing diagram of 15:2 compressor using 7:2 and 3:2 compressor .

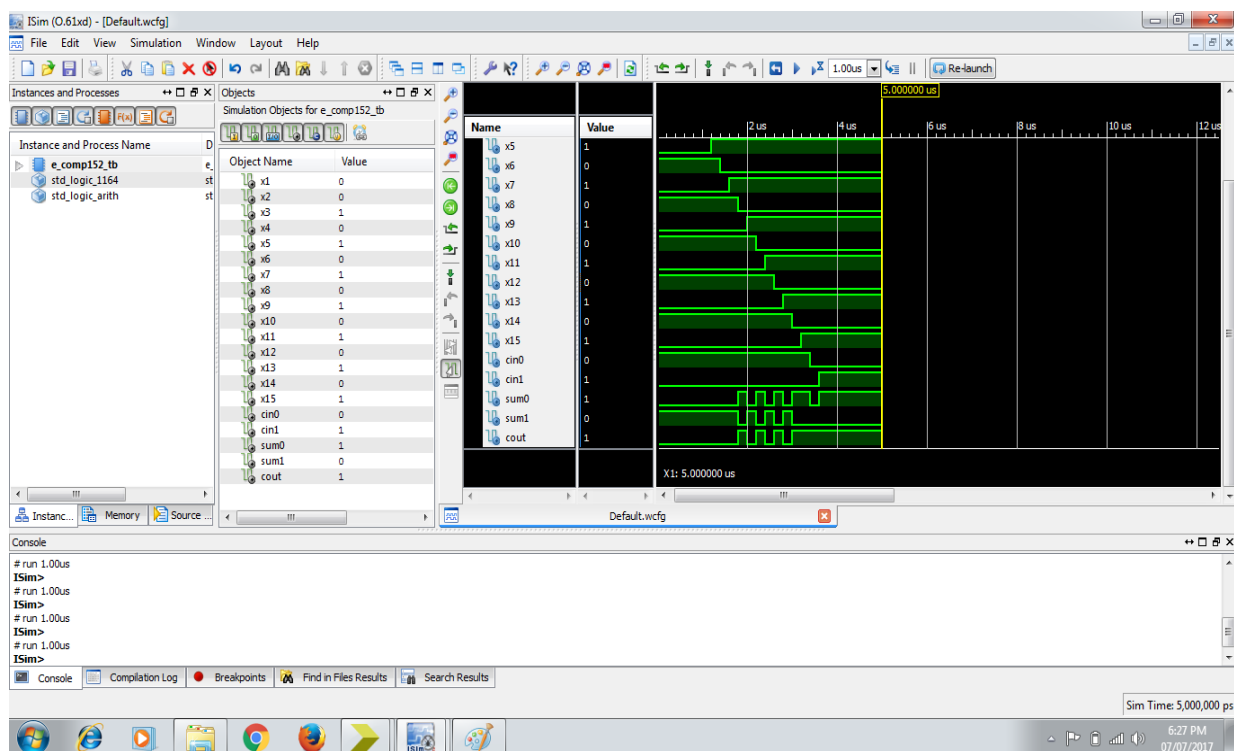


Figure 13 : Output waveform of 15:2 compressor

The multiplication of two 8 bit binary number i.e. a=01110111 and b=01110011 the output result is 001101011110101. following figure shows the delay of multiplier using compressor based urdwa tiryakbhayam Vedic multiplier with pipelining structure.

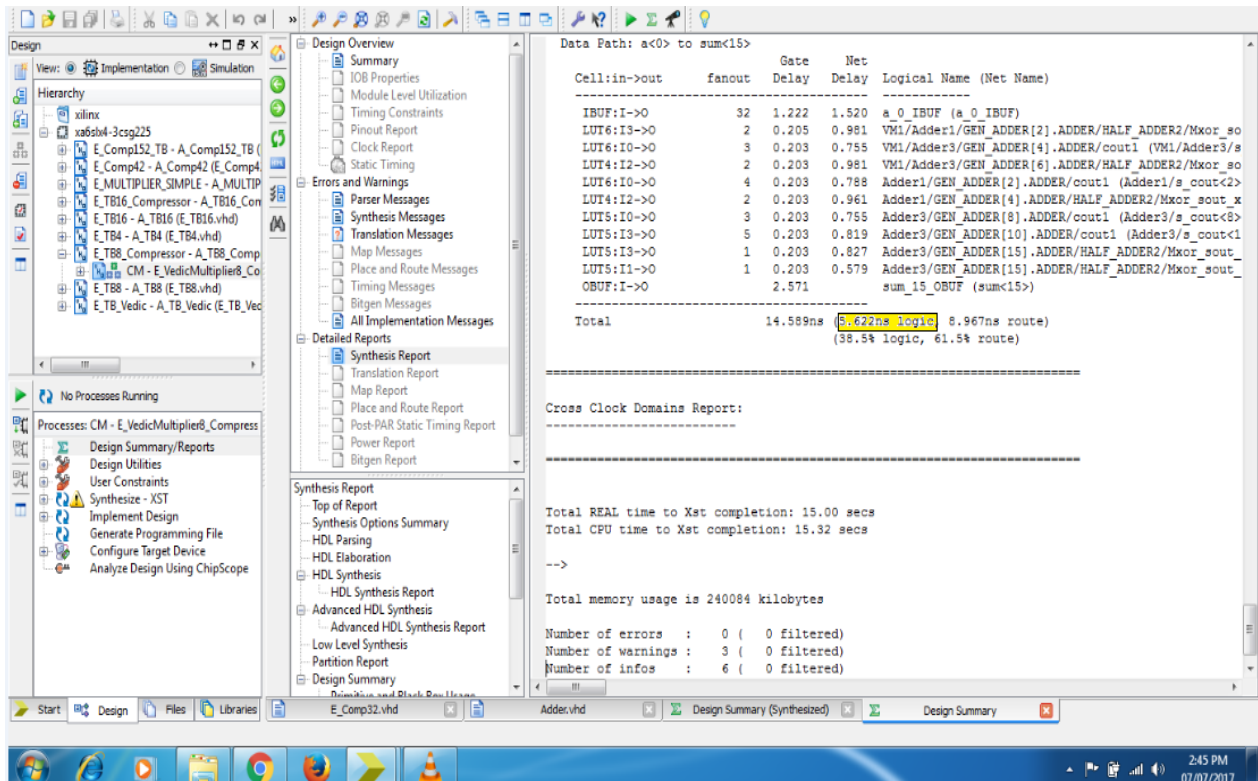


Figure 14: Analysis of delay in 8*8 bit multiplier

The power of implemented design can be calculated by Xilinx ISE Design Suite 13.2_1.

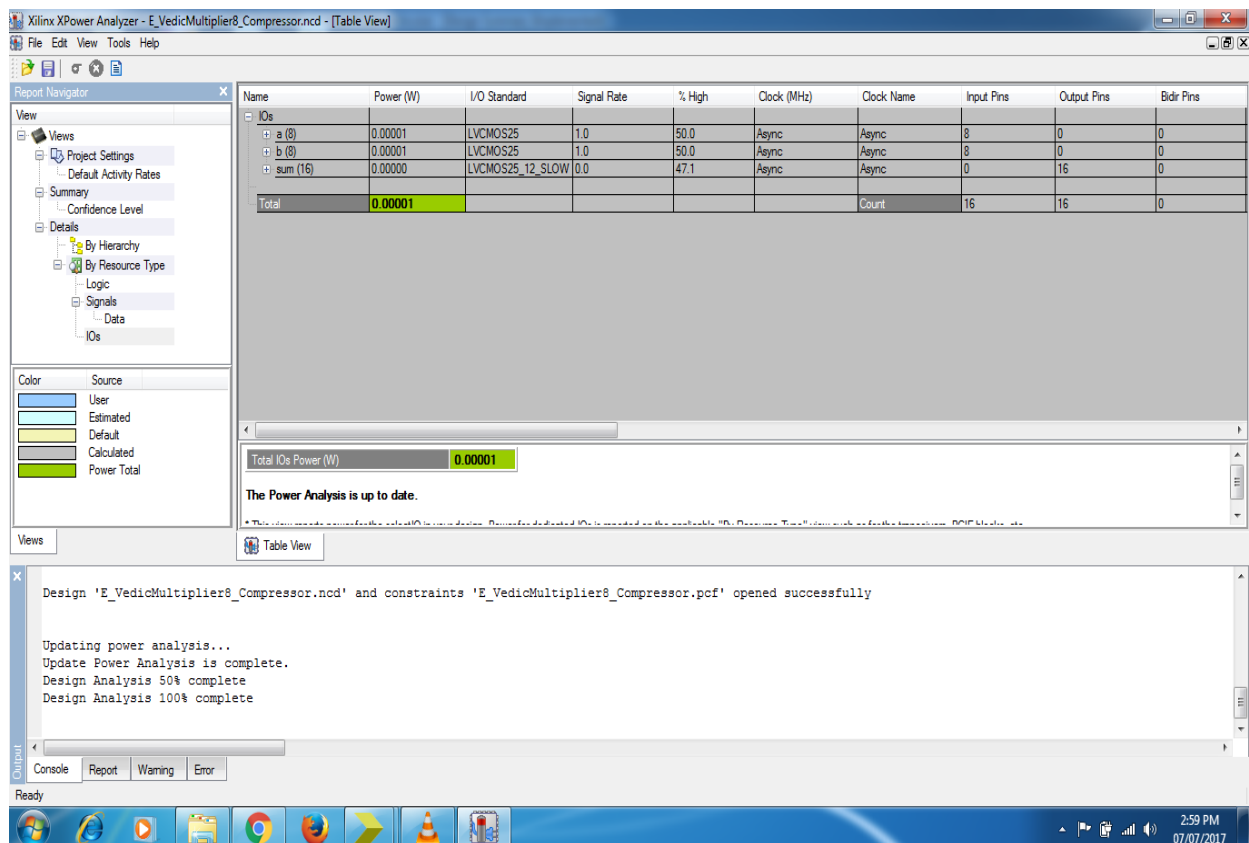


Figure 15: Analysis of output power in 8*8 bit Vedic multiplier

The RTL view of compressor based Urdhwa Tiryakbhyam multiplier using pipelining was shown in figure

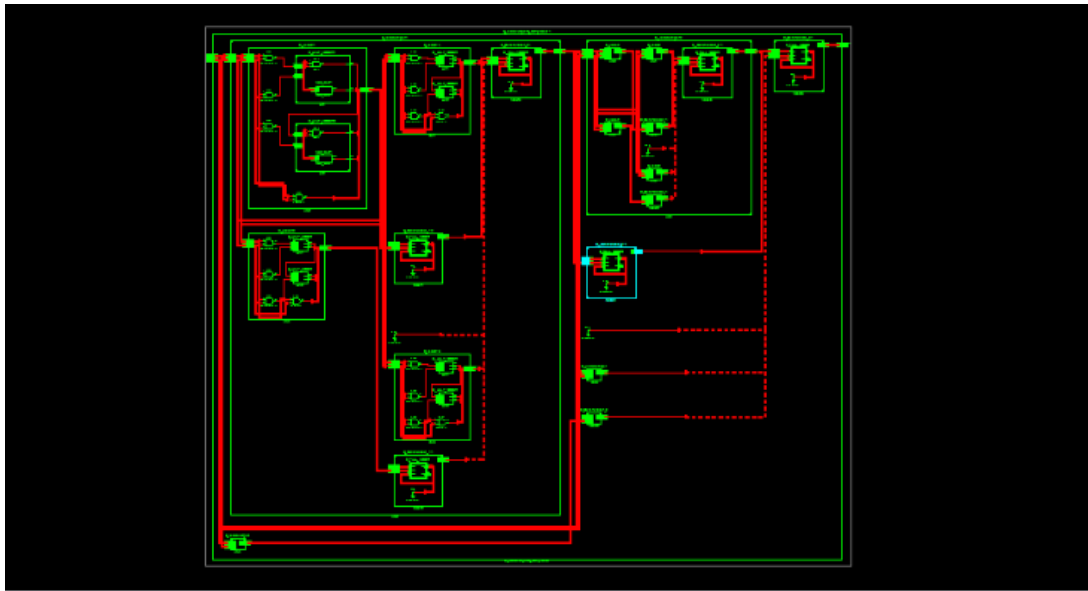


Figure 16: RTL view of 8*8 bit Vedic multiplier

V. CONCLUSION & FUTURE SCOPE

This is a not worthy change as for rapid multiplier design. Also, it can be seen that, a considerable lot of the stages have now been lessened to a negligible legitimate XOR operation, with an activity to decrease area. Hence from the vedic arithmetic, augmentation of two 8 bit numbers was created. At long last it is inferred that, the altered structure gives the better execution as far as speed and range. All these multiplier plans are planned utilizing VHDL. This process is done utilizing Xilinx 13.2-1 instrument for Spartan 6E. High speed data rates are achieved in pipeline based Vedic multiplier. Vedic multiplier using compressor based Urdhwa Tiryakbham with pipelining gives the fast operation and it reduces the delay and almost power constant.

As a future work the structure can be extended to 32 bit, 64 bit and to higher order bits multiplication. It can be concluded that Vedic multiplier is superior in all aspects like Speed, Delay, and Complexity. Multipliers are also very useful for DSP applications like FFT, Convolution, filtering etc. Ancient Vedic Mathematics gives efficient algorithms or formulae for multiplication. which increase the speed of devices. Urdhwa Tiryakbhyam is general mathematical formulae and equally works the best. It could be possible to implement a complete ALU using all these methods using Vedic mathematics methods. Vedic mathematics is long been known but has not been implemented in the DSP and ADSP processors employing large number of multiplications in calculating the various transforms like FFTs and control applications such as P, PI, PID Controller implementing in FPGA etc.

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