



Effect of Variability on Performance of CNFET Based Digital Circuits

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Abstract—Nowadays, Electronics trend is continuously reducing feature sizes, and employing continuously smaller components on integrated circuits, new challenges arise on the way of silicon CMOS circuits and devices. Emerging “Nano-devices” promise the possibility of increased integration density and reduced power consumption. The Carbon Nano-Tube (CNT) is one such device which is also the device of choice in this work. This work is concerned with building reliable systems out of these unreliable components. The work was done in HSPICE with the help of the Stanford CNFET model. By use of CNFET in logic gates, delay and power reduced by 4.14% and 28.19% respectively as compared to CMOS. By applying this technique on digital circuits we will improve the above results.

Keywords—CNFET, Power Delay Product, CMOS, Average Power, Delay.

I. INTRODUCTION

As technology scales down to 90nm, the bulk CMOS technology has approached the scaling limit due to the increased high power density, short-channel effects, severe process variations, increased leakage power dissipation, and so on. To discover this scaling limit, that has different types of materials are experimented. Now silicon MOSFET like CNFET has been produced to the replacement of the future Nano device electronics. The reason that makes CNFETs a promising gadget is that they are perfect with high dielectric steady materials and a remarkable 1-D band-structure that limits back-dissipating and makes close ballistic operation a practical plausibility. Utilizing this CNFET, a high-k door oxide can be sent for lower spillage streams while keeping the on-current drive capacity (contrasted with Si-MOSFET). CNFET has bring down short-channel impact and a higher sub limit slant than Silicon MOSFET [1].

In spite of this favorable improvement of CNFETs, CNFET only they can applied to a simple circuit like as ring oscillator, SRAM, etc. So because of the cost of the CNFETs is very high and furthermore issues of the fabrication with respect to limitation and fluctuation. That is the reason, the fabrication of carbon nanotube (CNT) at vast digital circuits on a single substrate has not been accomplished. For cost effective and solid use of CNFETs and the time gape has been decreased in exchanging from silicon MOSFET to CNFET innovation, the CNFET innovation has been required to be consolidated with minimal effort and dependable CMOS innovation.

II. BACKGROUND

Carbon filaments has the less than 10nm diameters has been first prepared in the 1970s by the decomposition of hydrocarbons through the synthesis of vapor grown carbon fibers at very high temperatures in presence of transition metal catalyst particles of less than 10nm in diameter [2, 3]. However, it was research publication which is Ijima's work in 1991 [4] that has been launched the field of Carbon Nanotubes.

III. LITERATURE SURVEY

“Performance evolution CNFET based Logic Gates” This paper presented power delay product and leakage power for the CNFET based gate are lower than the MOSFET based logic gates by 100 to 150 times.[5]

This paper “Carbon Nanotube Field-Effect Transistors and Logic Circuits” Presented that prospect for nano-tube is attractive but it is not realistic. Several issues need to be resolved. For example, as-grown nanotubes come in a mixture of semiconducting and metallic tubes. [6]

This paper “HSPICE Implementation of CNTFET Digital Gates” concluded that performed the basic digital gates using CNFET and also presented that this modelling of CNTFET and using this model, they designed various digital gates and designed for unipolar, MOSFET-like CNTFET devices. CNTFET technology provides more efficient way to implement these

functions in term of delay, power consumption and area. For designing of AND and OR gates, CMOS technology include SIX transistors, whereas CNTFET based circuits reduced by FOUR. [7]

IV. INTRODUCTIN OF CNFET

Depending upon the detailed arrangement of carbon atoms which is also known as the CNT chirality [Satio 98] can be either metallic (multi wall-CNT) or semiconducting (singled wall-CNT). MWCNTs has the zero or very little energy gap so they are undesirable for transistor applications. On the other hand s-CNT, can be used to generate or create Carbon Nanotube Field Effect Transistors (CNFETs).

To assemble the electronic device CNFET which can be employed by semiconducting single-wall carbon nanotubes, and the SWCNFET is obtained by the replacing the channel of a conventional MOSFET with CNT as shown in figure 1. Now the depends on the angle (which can shows that the as a chirality integer vector (n, m) of the atom arrangement along with the nanotube can be either metallic or a semiconducting. The When $(n=m)$ or the $(n-m = \text{"* of 3"})$ then the tube is metallic otherwise the tube is semiconducting.

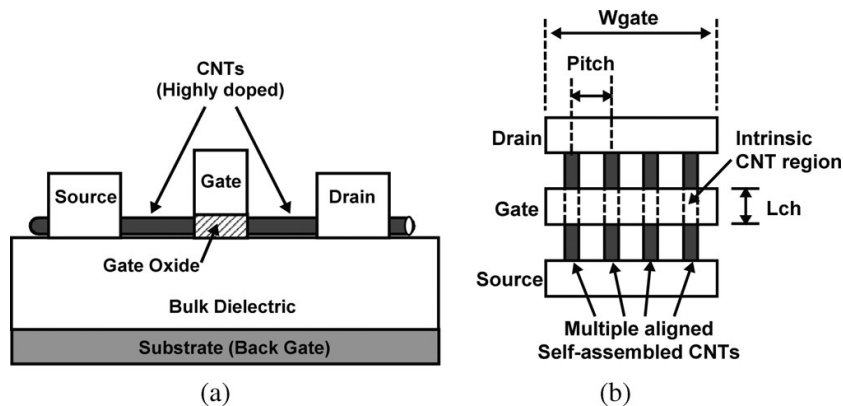


FIGURE 1 CNFET Model (a) Cross Section View (b) Top View

As shown is above figure which is shows that the top gated CNFET has been shown and it is fabricated on the oxide silicon SI substrate so that can be used as a back-gate in the CNFET. In past 1990s, most of the CNFET has been studied and adopted a back gate of top content structure which can be shown in the research paper [8], [5], in which the nanotubes has been grown in the conduction substrate by covered an insulating layer. In the nanotube device there are two metal contacts are deposited to serve as a source and drain electrode while the conduction substrate is the gate electrode in the three-terminal devise.

Few years ago CNFET are found to have a poor devise characteristics likewise an am bipolar transistor characteristics and second one is the gentle sub threshold swing. So to improve the bad devise characteristics, the dual gate CNFET structure have been proposed. This structures show a MOSFET like a unipolar transistor characteristic, excellent sub threshold slopes, and a drastically improved off state. Each and every device has one or more single-wall semiconducting CNT. So in this CNT the current can be controlled device by the varies the device the parameters such as the gate length, last pitch between nanotubes and the last was an number of nanotubes [10].

2.1 Structure of CNFET

A thick silicon dioxide film can be covered on a silicon wafer and then it is going to the fabricated using a two different material which is gold as well as platinum electrode in standard semiconductor manufacturing process. So after that the carbon nanotube is then introduced as a channel as between source terminal and drain terminals [11].

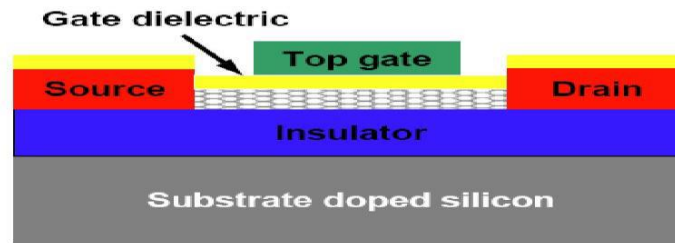


FIGURE 2 Structure of CNFET

The under the silicon wafer there has a heavily doped with has the impurities makes it good conductor which can be act as a gate terminal. By applying the appropriate voltage to the gate terminal of the nanotube which is either on or off. But the first CNTFET were proposed or reported in 1992 which can be shown in figure 2. There are different types of the Carbon nanotube, but carbon nanotube geometries may be grouped in the two major categories which first one is the planner and the second one is the coaxial CNTFET. In the terms of the device operation CNFET can be different types which is Schottky Barrier (SB) controlled FET (SB-CNFET) or MOSFET like FET.

2.2 Calculation of Average Power

- Equation for average power = $C_{Load} \cdot V_{dd}^2 / T$
- “.measure pwr AVG P(VDD) FROM 0NS TO 90NS”
- By use of this statement, we can find power in .mt0 file

V. SIMULATION RESULT OF INVERTER USING CMOS AND CNFET

The function of not gate is invert the input from low to high and high to low. By applying transient analysis we received this output. The axis of this graph y-> x is voltage -> time. Due to C_{load} the delay involved in output.

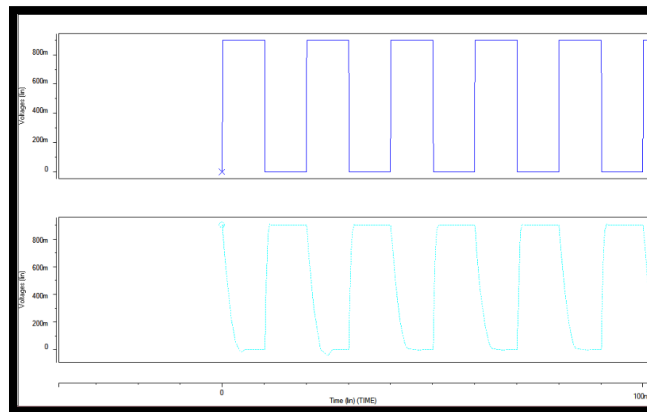


FIGURE 3 Simulation Result of INVERTER using CMOS

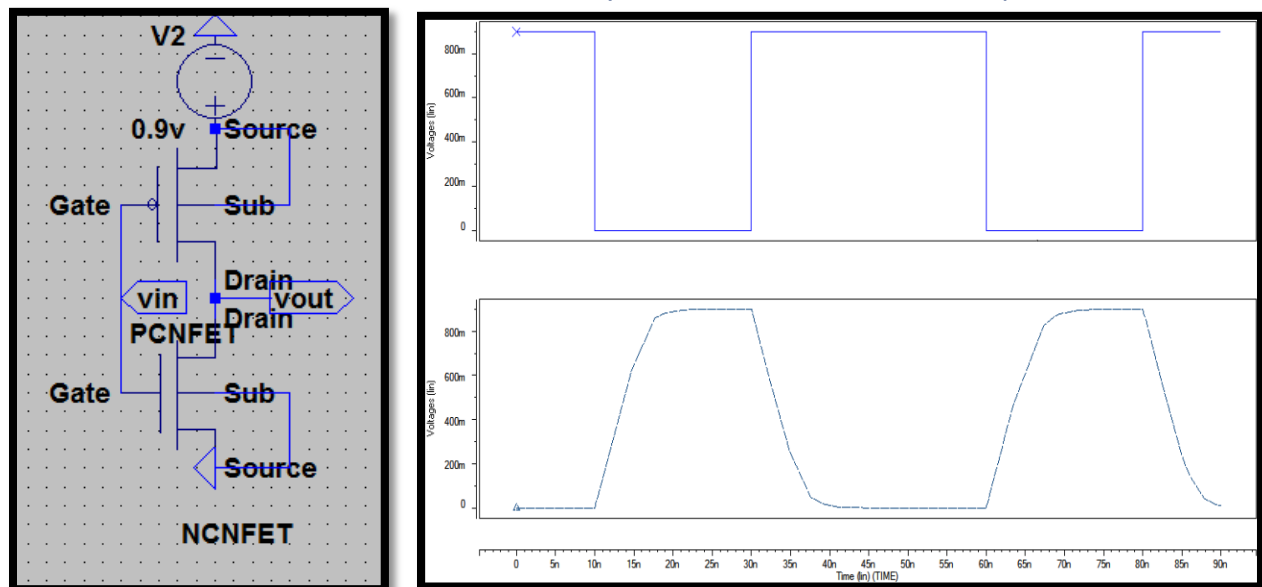


FIGURE 4 Simulation Result of INVERTER using CNFET

VI. SIMULATION RESULT OF NAND GATE USING CMOS AND CNFET

The function of NAND is when both are high then output will be high and rest of the cases output will be low. By applying transient analysis we achieved output which is shown as below. The axis of this graph y-> x is voltage -> time.

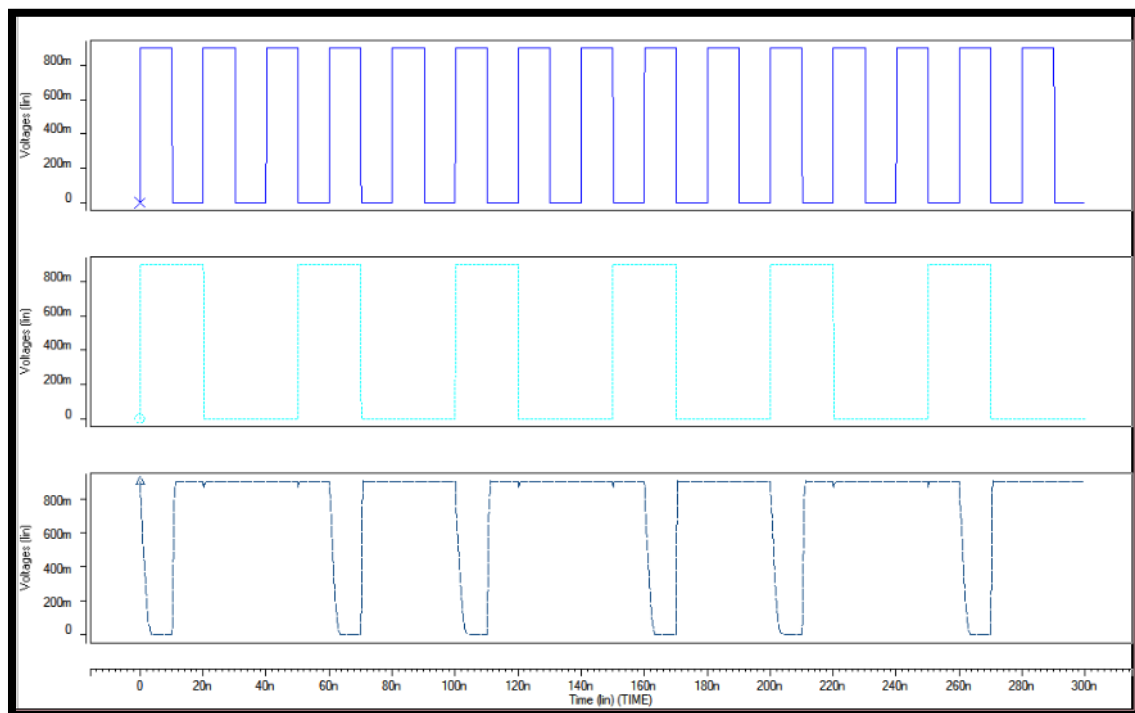


FIGURE 5 Simulation Result of NAND Gate Using CMOS

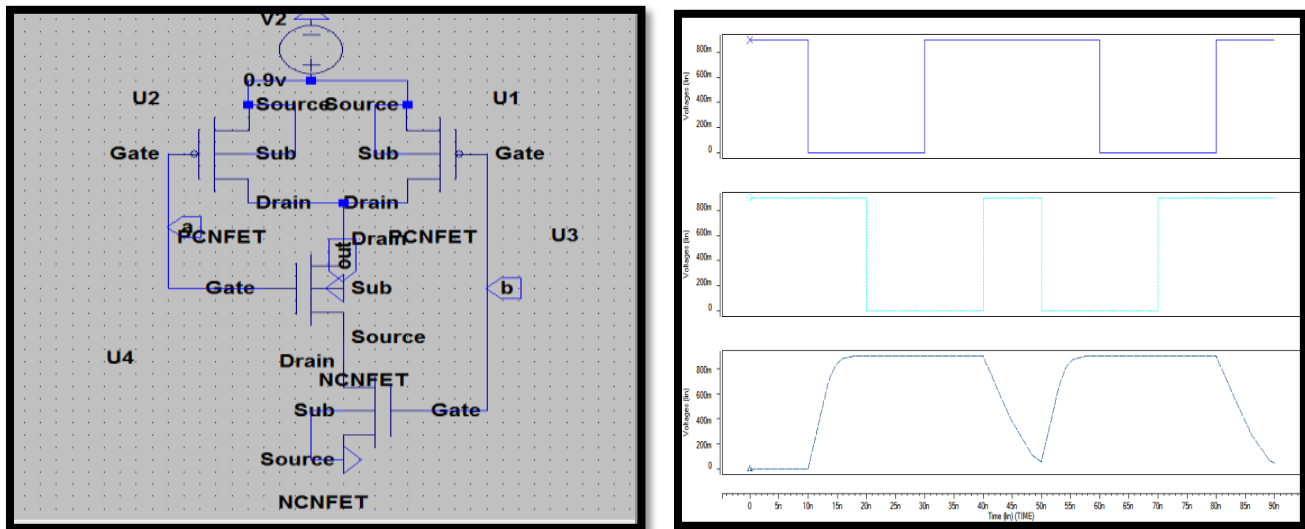


FIGURE 6 Simulation Result of NAND Gate Using CNFET

VII. COMPARISON TABLE OF ALL GATES USING MOSFET

Parameters	NOT Gate	NAND Gate	NOR Gate	XOR Gate	Half Adder	Full Adder	4 Bit Full Adder
Propagation Delay(Sec)	2.865e-10	2.64e-08	4.839e-10	14.88e-10	28.87e-10	1.316e-8	4.546e-8
Power(w)	3.935e-06	1.645e-06	2.445e-06	8.923e-05	9.245e-05	4.950e-05	5.024e-05
PDP(J)	1.127e-17	4.342e-14	11.83e-16	13.28e-16	2.66e-17	6.52e-13	2.283e-14
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IX. CONCLUSION

After facing the limitation of CMOS, we have to switch on another material that is CNFET. Model design of both is same, but MOSFET gate is replace by Carbon Nano Tube. This work done using standard Stanford model 32nm and operating supply voltage is 0.9V. After completion of simulation, the conclusion is shown in tables. Here we can see both the table with same supply voltage and same technology file. By use of CNFET in logic gates, delay and power reduced by 4.14% and 28.19% respectively as compared to CMOS.

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