



Design of Low Power DRAM in 90nm Technology

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Abstract — The semiconductor industry is trying to catch up with Moore's law by scaling the devices namely microprocessor and memories. Reduction in size guarantees reduction of its parasitic mainly capacitance. The parasitic mainly contribute to increment of size and unnecessary power dissipation in the overall device as a well designed layout of chip ensures quality of work and better performance. Memories are circuits or systems that store digital information in large quantity. This paper is on the analysis and design of CMOS. Memories namely DRAM and associated peripheral circuits. Semiconductor memory is classified on the basis of functionality, access patterns and nature of storage mechanism. Then, we shall move into some proposed models, which have more functional advantages with respect to data retention stability, power consumption, leakage power etc. Briefing of the functioning of the circuits along with issues and benefits will be done in the following matter. To implement circuits, software named Digital Schematic (DSCH) editor will be effectively used. This software has the ability to automatically generate Verilog code. Micro Wind is another software which we will need to perform power analysis, which uses automation to form layouts of the circuits and subsequently, determining the layout area and power dissipation.

Keywords- Cell, Power Dissipation, Scalable, CMOS, leakage current, etc.

I. INTRODUCTION

Dynamic Random Access Memory (DRAM) devices are used in a wide range of electronics applications. Although they are produced in many sizes and sold in a variety of packages, their overall operation is essentially the same. DRAMs are designed for the sole purpose of storing data. The only valid operations on a memory device are reading the data stored in the device, writing (or storing) data in the device, and refreshing the data periodically. To improve efficiency and speed, a number of methods for reading and writing the memory have been developed. Dynamic random access memory (DRAM) integrated circuits (ICs) have existed for more than twenty-five years. DRAMs evolved from the earliest 1-kilobit (Kb) generation to the recent 1-gigabit (Gb) generation through advances in both semiconductor process and circuit design technology.

Tremendous advances in process technology have dramatically reduced feature size, permitting ever higher levels of integration. These increases in integration have been accompanied by major improvements in component yield to ensure that overall process solutions remain cost-effective and competitive. Technology improvements, however, are not limited to semiconductor processing. Many of the advances in process technology have been accompanied or enabled by advances in circuit design technology.

Complementary metal oxide semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. CMOS is also sometimes referred to as complementary symmetry metal oxide semiconductor (or CMOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

II. LITERATURE SURVEY

Scaling-down has been the conventionally effective method to grow DRAM chip capacity, to reduce power consumption and to lower the per-bit cost. As scaling down, DRAM cell shape been shrinking to smaller dimensions, which results in size reduction of access transistor, storage capacitor and peripheral circuits. Firstly, smaller capacitor translates into a lower capacitance, reducing the stored charge; secondly, scaled DRAMs applies lower supply voltage, which further decreases per-cell charge and also increases the gate induced drain leakage; meanwhile, at smaller dimensions, adjacent cells are likely to electrically disturb each other; moreover, smaller cell geometry increases the resistance on both access

transistor and bit line, obstructing the cell charging process. In addition to charge decrease, the input offset voltage on the sense amplifiers is also expected to increase, which makes it more difficult to sense data.

Moreover, scaling to smaller technology nodes grow the fabrication complexity and makes it more difficult to precisely control the dimensions of DRAM cells, which introduces more severe process variations (PV). Accordingly, DRAM cells are expected to show more statistical behaviors in a wide range; and, such uncertainty might cause increasingly more cells to violate the design specifications, which is beyond the tolerance of existing mechanisms such as row/column redundancy.

III. PROPOSED SYSTEM AND METHODOLOGY

Constructing a highly scalable and dense main memory subsystem with large access bandwidth has become a major challenge for modern computing systems. Traditional memory technologies, like DRAM and NAND Flash, suffer from either poor scalability or limited access bandwidth. Recent studies have identified emerging Phase Change Memory (PCM) as one of the most promising low power main memory technology candidates, because of its short read latency and good scalability. However, PCM still faces serious write disturbance problem below 20nm technology. Write disturbance leads to more cell programming errors, and thus degrades write reliability. Simple solutions, such as allocating large inter-cell space and adopting strong error correction code (ECC), either reduce memory density or incur large performance overhead. In this paper, we propose DIN, a Data encoding based Insulation technique, to mitigate write disturbance in highly dense PCMs. DIN improves memory density by eliminating inter-cell thermal band along a word line. The non-negligible disturbance errors, are then minimized by disturbance-aware data encoding, based on how PCM cells are programmed at device level. Our experimental results show that DIN gains write disturbance resistance in high density PCM chips while achieving comparable performance for a wide range of applications.

Figure 1 (a) shows the structure of 2T1D and 3T1D and Figure 1 (b) shows the structure of an N-type gated diode. In Figure 1 (a), both 2T1D and 3T1D cells have dual bit-lines. BLw is the write bit-line signal and BLr is the read bit-line signal. These two structures are composed of one write access gate (wg), one read access gate (rg) and one gated diode (gd). The 3T1D structure has an extra read select gate (rs). Gates wg and rs are controlled by WLw and WLr respectively. WLw is the write word-line signal and WLr is the read word-line signal. Gated diode gd can be implemented using a transistor in which only the gate and source of the transistor is used and the drain is not used as shown in the middle of Figure 1 (b) or all three of gate, source and drain are used but the source and drain are connected together to form two diodes in parallel [2] as shown in the right hand side of Figure 1 (b).

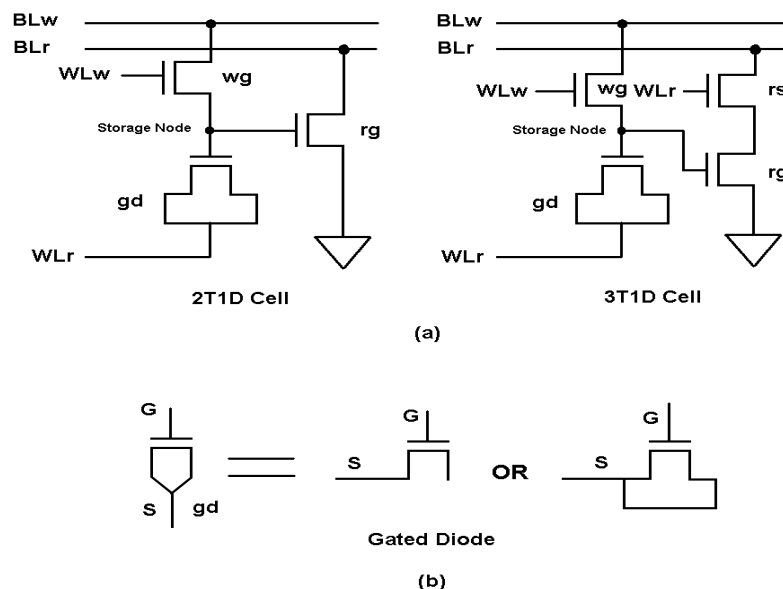
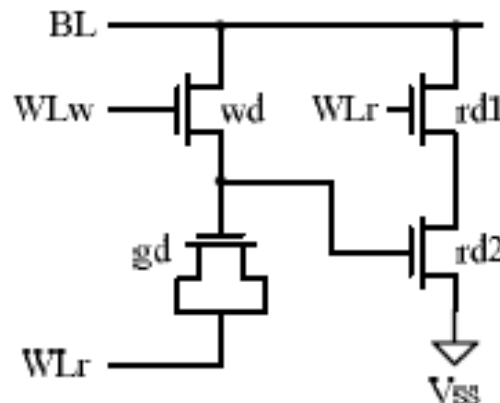


Figure 1. (a) 2T1D and 3T1D structure. (b) Gated diode structure.

IV. WORKING PRINCIPLE

As the name DRAM, or dynamic random access memory, implies, this form of memory technology is a type of random access memory. It stores each bit of data on a small capacitor within the memory cell. The capacitor can be either charged or discharged and this provides the two states, "1" or "0" for the cell. It may appear that the refresh circuitry required for DRAM memory would over complicate the overall memory circuit making it more expensive. However it is found that DRAM the additional circuitry is not a major concern if it can be integrated into the memory chip itself. It is also found that DRAM memory is much cheaper and has a much greater capacity than the other major contender which might be Static RAM (SRAM).

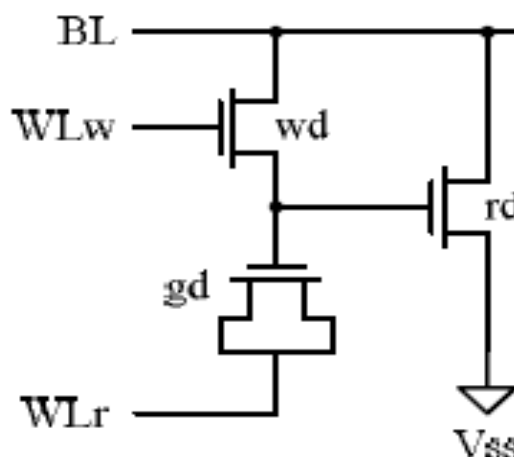
- **Typical 3T1D memory cell**



Typical 3T1D Memory Cell

Fig. shows the typical 3T1D memory cell. The 3T1D memory cell consists a write access transistor (wd), a read access transistor (rd1), a read select transistor (rd2), and a gated diode (gd) for data storage. Writing and reading operations are similar to those of 2T1D cells. Compared to 2T1D memory cell, 3T1D memory cell has higher gate overdrive for speed improvement as the source of rg is biased lower. Moreover, 3T1Dmemory cell consumes less power due to the fact that rs cuts off short current path from BL to VSS when the word is off. The disadvantage of 3T1D memory cell is its cell size, with one additional transistor for each cell compared to 2T1D cell.

- **Typical 2T1D memory**

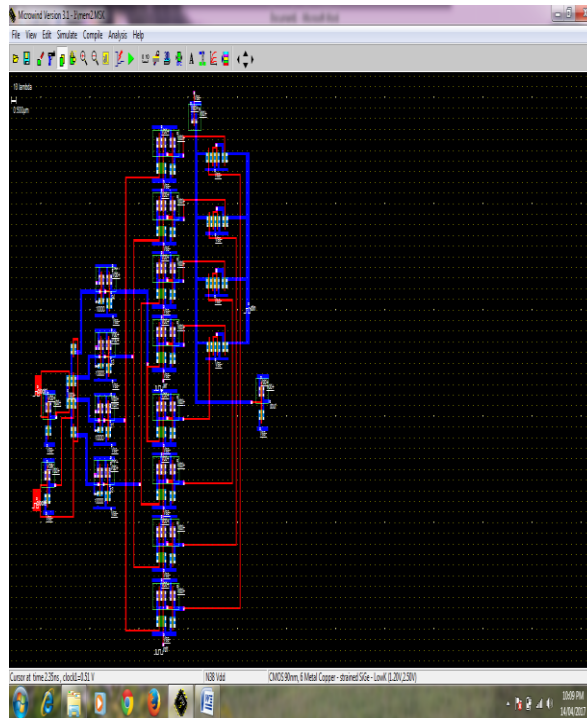


Typical 2T1D Memory Cell

Fig. shows the typical 2T1D memory cell. The 2T1D memory cell consists a write access transistor (wd), a read access transistor (rd), and a gated diode (gd) for data storage. During a writing operation, WLw raises high and WLr remains low, data is written into gd from BL via wg, low for 0-data and high for 1-data. During a reading operation, WLr is pulsed from low to high, producing a relatively large voltage swing on the gate of gd and turning on rg if 1-data is stored; whereas for 0-data, there is a relatively small voltage swing on the gate of gd, and rg remains off. As a result, due to the

nonlinear capacitance characteristic of the gated diode, proper control of the threshold of r_g , and voltage boosting, fast access, high noise margin, and low-voltage operation could be obtained.

Layout of 2T 1D DRAM CELL



The overall layout is configuring using the different combination of the NAND and Inverter cell. The first stage is consisting of two inverter connected in series with the input as CLK 1 and CLK 2. 2:4 decoder is used to produced the four output for the next consecutive stage. Boost up circuit is for the recovery of the transition time delay occurs during the operation. Read/ write logic having 8 cell with the combination of the NAND and inverter cell, which splits up in four cells for write and remaining for the read cell. The output of read/write logic is given to the DRAM driver circuit, but operation of DRAM driver is decided by the Din clk. And the final output is given to the output stage of final inverter circuit.

Final result of 2T 1D DRAM cell



Figure : Input/ output waveform of DRAM cell

V. CONCLUSAION

The 2T-1D DRAM cell is an attractive alternative to conventional 3T-1D cells for next generation on chip memory designs since they offer better tolerance to process variations that impact performance, cell stability, and leakage power. From the above results of power calculation of 2T-1D DRAM Cell of the different technologies, it is observed that power consumption increases as length and width of the transistor decreases. It is because when the aspect ratio of MOS decreases the gate loses control over the current, hence the overall power consumption increases. Also after simulating schematic design in DSCH tool and layout in Microwind it is observed that digital technology gives less power dissipation as compared to analog technology. Also after applying process variation on 2T-1D DRAM cell power get decreases as technology get decreases with respect to applying voltage.

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