

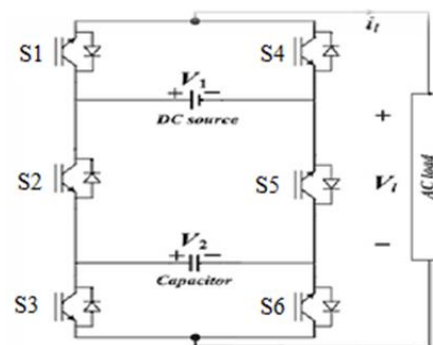
**Voltage Control Based Five-Level Packed U-Cell Inverter**Sakthivel A¹, Vikniswaran M², Selva Bharathi V³, Vikash B⁴Assistant Professor, Electronics and Electrical Dept, Dr. Mahalingam College of Engineering and Technology, Pollachi¹UG Student, Electronics and Electrical Dept, Dr. Mahalingam College of Engineering and Technology, Pollachi²UG Student, Electronics and Electrical Dept, Dr. Mahalingam College of Engineering and Technology, Pollachi³UG Student, Electronics and Electrical Dept, Dr. Mahalingam College of Engineering and Technology, Pollachi⁴Mail id: vikkiaharendra@gmail.com , selvamcet320@gmail.com , b.vikash007@gmail.com

Abstract — The multilevel inverters are widely used because of its more advantages. Therefore a voltage control based five-level packed U-cell inverter is introduced incorporating the least number of switches and DC sources, hereby ensuring the low switching losses. Here sensor-less voltage control based on redundant switching state is proposed in this paper.

Keywords- Multilevel ; Voltage control ; Five-level ; Packed U-cell ; Switching losses ; Sensor-less ; DC (Direct Current) source ; Redundant switching states.

I. INTRODUCTION

The inverter is an electric device that converts direct current (DC) to alternate current (AC). These inverters are used in backup power in home, office, industries and aircraft. A multi-level inverter is a type of inverter technology which is capable to provide desired alternating voltage level at the output using multiple lower level direct current (DC) voltage as input. There are several multi-level topologies are available such as cascaded H-bridge, Diode clamped and Flying capacitor multi-level inverters. In this proposed inverter topology self-voltage based sensor-less operation is proposed. Switching algorithm for this inverter topology is simulated using MATLAB.

II. PROPOSED INVERTER TOPOLOGY**Figure 1. Circuit diagram of the proposed topology**

In this project proposed topology eight switches can provide eight switching states can provide different paths for current. This proposed topology has the ability to operate as five-level inverter.

The various switching states for this proposed switching algorithm is shown in below Table 1.

States	S1	S2	S3	S4	S5	S6	O/P	V_t
1	1	0	0	0	1	1	V_1	$+2E$
2	1	0	1	0	1	0	$V_1 - V_2$	$+E$
3	1	1	0	0	0	1	c	$+E$
4	1	1	1	0	0	0	0	0
5	0	0	0	1	1	1	0	0
6	0	0	1	1	1	0	$-V_2$	$-E$
7	0	1	1	1	0	0	$V_2 - V_1$	$-E$
8	0	1	1	1	0	0	$-V_1$	$-2E$

Table 1. Switching states

Here in this proposed inverter topology capacitor voltage is fixed as half of the direct current (DC) source voltage assumed as 'E' as shown in Table 1 and Figure 1 and also assume the source voltage as 'E'. It is clear that the existing eight switching state can able to produce five-level output voltage.

2.1 Conducting paths and switching states

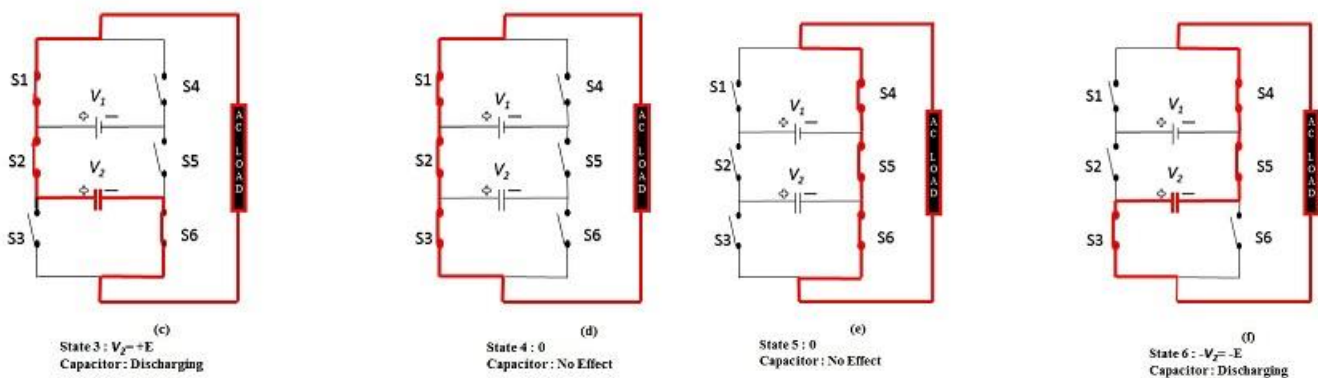
The capacitor states for various switching states are shown in Table 2. Capacitor is charging during positive half cycle and discharging during negative half cycle.

State	Capacitor State
1	No Effect
2	Charging
3	Discharging
4	No effect
5	No effect
6	Discharging
7	Charging
8	No Effect

Table 2. Capacitor voltage states

One of the main problem in multi-level inverter is balancing the capacitor voltage is high switching frequency and complexity of the controller. Since the voltage control based packed U-cell inverter has redundant switching states and also voltage balancing of capacitor also integrated into the modulation network.

The main advantage of this topology is without any sensor or controller the capacitor voltage is balanced with the redundant switching states. The capacitor is designed to only charge to half of the direct current (DC) source amplitude.



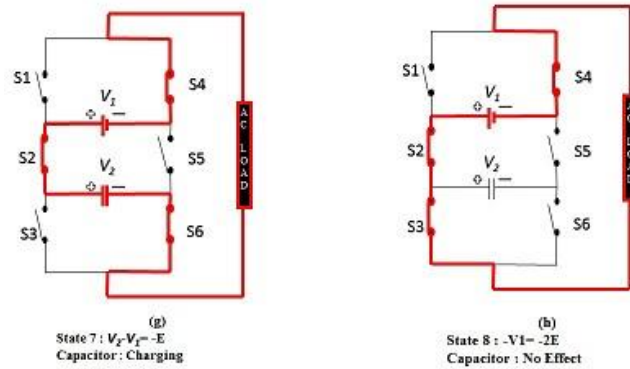


Figure 2. Conducting paths and switching states

The conducting paths and switching states of proposed five-level inverter topology is shown in figure 2. The capacitor states for various switching states also mentioned in figure 2.

Where V_1 is applied voltage, V_2 is voltage across capacitor, S1-S6 IGBT switches and V_t is output voltage.

Based on states (2) and (7), it is cleared that the capacitor is charged when it is connected in series with the source and load. While the source voltage is fixed at $2E$, the capacitor must be charged up to the E as indicated for to produce proper output voltage.

2.2 Open-loop switching algorithm for proposed inverter

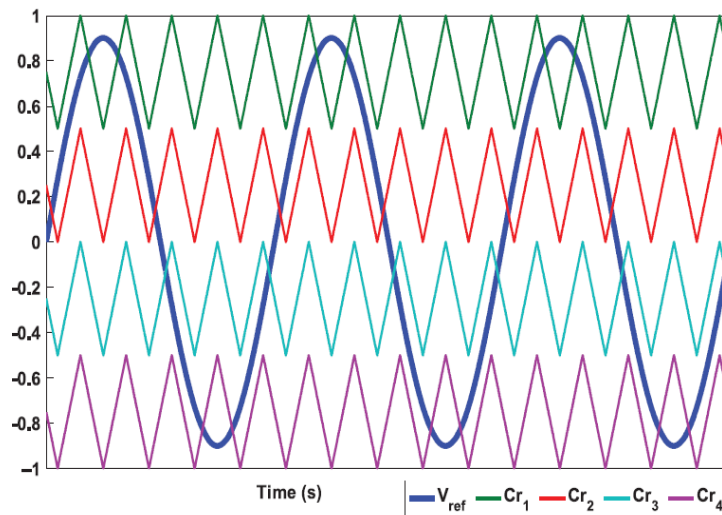


Figure 3. Vertically shifted carrier waveform

Five-level inverter including four carrier waves and sinusoidal reference waveform is used for this open-loop algorithm. The firing pulses associated with switching states 1, 2, 3, 4, 5, 6, and 8 are generated based on comparing V_{ref} with four carrier waveforms. If V_{ref} is positive, then state 4 will be used to produce zero level at the output. When V_{ref} is negative, the output zero-level voltage will be generated by state 5. The vertically shifted carrier waveform is shown in figure 3.

Where, Cr_1 , Cr_2 , Cr_3 , Cr_4 -reference carrier waveform,

V_{ref} - Reference Voltage.

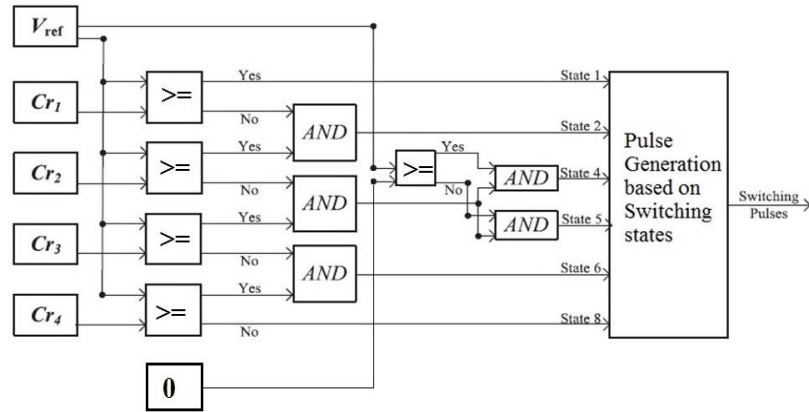


Figure 3. Open-loop switching algorithm

By applying this proposed algorithm on packed U-cell inverter generates five-level voltage waveform at the output without any voltage sensors in this controller. The described algorithm is shown in figure 4. The proposed algorithm technique does not depend on system sensors, switching frequency and grid frequency. It can operate without any sensors.

III. SIMULATION RESULTS

The voltage control based five-level packed U-cell inverter is designed with MATLAB simulation file and it is simulated. The proposed algorithm topology is verified with this simulation file.

The output voltage and current waveform of the voltage control based five-level packed U-cell inverter by obtaining simulation is shown in figure 5. This output waveforms which is obtained by the simulation is concluded clearly that the proposed algorithm is able to produce the five-level output voltage.

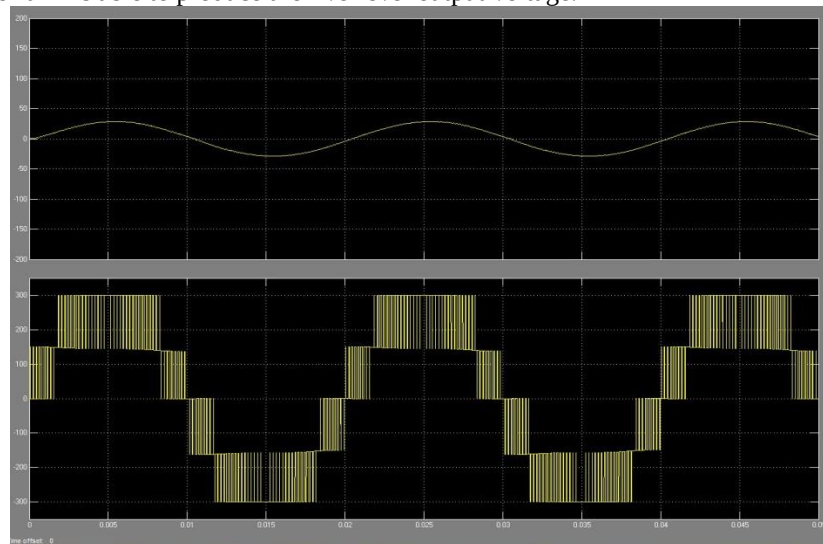


Figure 5. Output voltage and current waveform

By obtaining the above given waveform it is being concluded clearly that the proposed algorithm is able to produce the five-level output voltage and the five levels are basically given as $[+2E, E, 0, -E, -2E]$. Here the input direct current (DC) Voltage is given as the source and it is as of 300V and capacitor voltage is being defined as proposed that is half of the source voltage 150V. In figure 5 current level is between +30 to -30 and voltage is 300, 150, 0, -150, -300.

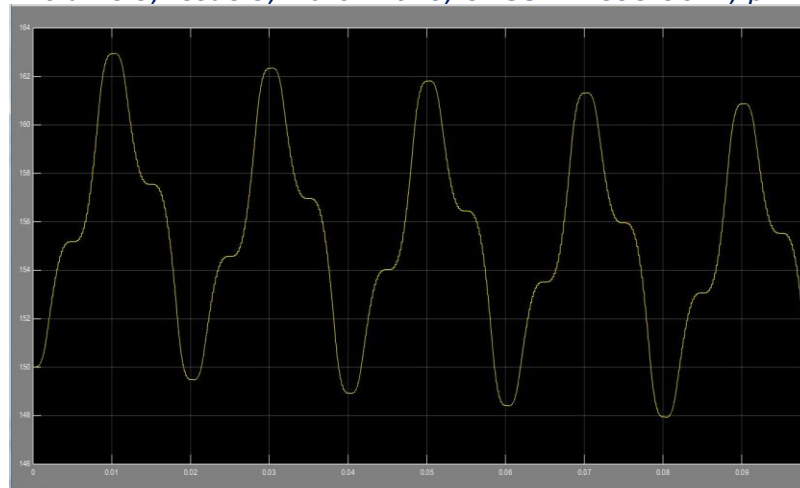


Figure 6. Capacitor voltage tracking waveform

The figure 6 shows the voltage tracking waveform of capacitor. This waveform clearly shows that the self-voltage balancing technique is used and it is proved that the voltage across capacitor is controlled without any external controller.

IV. CONCLUSION

Thus the voltage controlled based five-level packed U-cell inverter is being simulated using MATLAB simulation. This inverter can effectively increase the number of output voltage levels with a single voltage source. The capacitor voltage is balanced without involving any external controller or sensor. The proposed sensor-less voltage controller has been integrated switching technique to work as open-loop system. The obtained current level is between +30 to -30 and voltage level is 300,150,0,-150,-300. By FFT analysis the level of harmonics produced for the proposed voltage control based five-level packed U-cell inverter is 2.71 %.

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