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A 16-bit Booth Multiplier Design Using GDI Logic Style

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Abstract

Gate Diffusion input (GDI) is a newest technology of designing a low power digital combinational circuit is described. This method allows reduce power consumption, Delay and area of any digital circuits while maintain low complexity of logic design. The GDI allow implementing of a wide range of complex logic function using only two transistors. This technique is prefer for designing fast using less number of transistors while improving logic level for swing and static power characteristics and also allows simple design by using smaller cell library. Comparision of GDI transistor count with CMOS and also Compare Power consumption and delay. Simulation result shows that the propose GDI has been good performance in compared to CMOS design

In this paper, the 16-bit Booth multiplier is design based on GDI and the simulations are performed by TANNER TOOL based on 45nm GDI logic.

Keywords: *Booth Multiplier, GDI logic, CMOS technique, 45nm technology, TANNER EDA simulation result*

I. INTRODUCTION:

In Arithmetic circuit, likes multiplier different adders, are one of the basic components in the design of any communication circuit. Therefore Digital multipliers are most commonly used in many digital circuit designs. They are very fast, most reliable and efficient component that is utilized to implement any operation. The power dissipation in a multiplier is a very important issue as it reflects the total power dissipated by the circuit and hence affects the performance for the device. Most of digital signal processing (DSP) systems incorporate a multiplication unit to implement algorithms such as correlations, convolution, and filtering and frequency analysis. Multipliers are key components of many high performance systems such as FIR filters, microprocessors, DSP processors, etc

This paper focuses on Booth Multiplier algorithm, which is suitable for high- speed and low-power applications. The algorithm is symmetric for binary Multiplication due to the interchangeability of the multiplicand and the multiplier.

Proposed System Gate Diffusion Input (GDI) a new technique of designing a low-power digital combinational circuit is described. This technique allows reducing power consumption, propagation delay and area of digital circuits while maintaining low complexity of logic design. The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. Comparison of GDI result with CMOS is presented.

II. Architecture of Multiplier

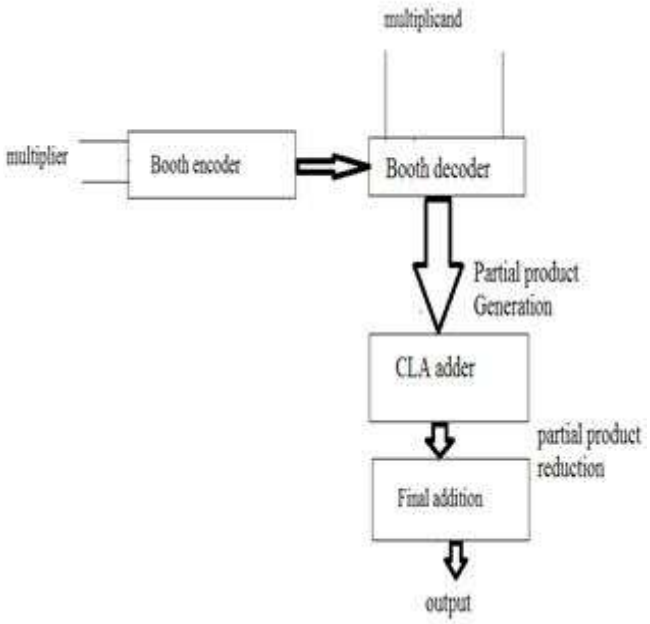


Figure 1: Multiplier Architecture

(A) Booth Encoder

Booth encoder is the essential part of the Multiplier. It consumes much of the area of Multiplier. The booth encoder can be designed in various ways. As much as good the booth encoder the number of getting output chances good. Booth encoder is implemented with the help of inverter, XOR and AND gates. It will generate the three control signals which are given to the booth decoder for the generation of the partial product. According to the design of booth encoder and will get the output of three control signals Direction (Dm), Shift (Sm), Addition (Am)

Direction find out whether the multiplicand was positive or negative, Shift explained whether the multiplication operation include shifting or not and Addition explained whether the multiplicand was added to partial product. The expression for booth encoder as shown as below

Direction, Dm= ai+1

Shift, Sm= ai-1 AND (ai+1 XOR ai) OR ai-1' AND (ai+1 XOR ai)

= ai+1 XOR ai

Addition, Am= ai-1 XOR ai

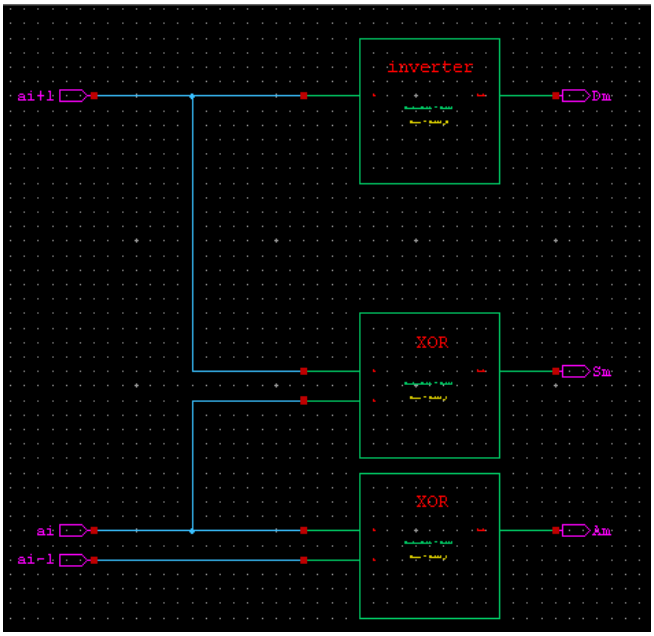


Figure 2: Booth encoder

(B) Booth decoder

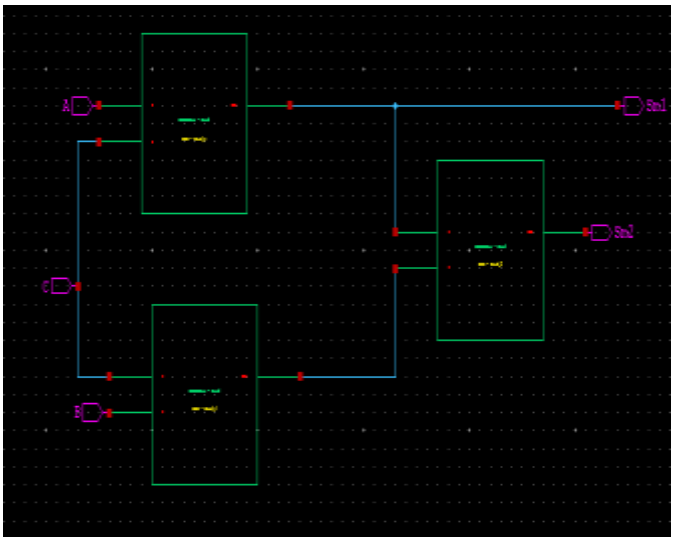


Figure 3: Booth decoder

Booth encoder generates the selector signals which are given to the booth decoder. Also the Y no. of inputs are applied to the booth decoder. It can be design in number of ways. Here actually used the multiplexer for the complete designing of booth decoder. With each output generated, simultaneously one bit half adder also put in front of every output of booth decoder because of generating the partial product.

The decoder block generates the partial product from the selector signals that they are generated in encoder block. This is the logic for the 1bit decoder that generates 1 bit of the partial product:

PPG = (ai●b1●-b2+ai-1●b1●b2) xor neg

(C) Carry Look-ahead Adder:

Adder is widely used in the generic computer because it is very important for adding data in the processor. The simplest binary adder is Ripple carry adder. It is easy to be understood and implemented. A more complex binary adder is Carry Look ahead Adder (CLA). It uses the same Carry Look ahead circuits to construct the higher-bit CLA recursively. It is widely used due to its superior performance over Ripple carry adder. The speed of execution is the most important factor that needs to be considered for appraising the quality of an adder. Traditional CLA is constructed by XOR, AND, and OR gates.

As seen in the Ripple-carry adder, its limiting factor is the time which takes to propagate the carry. The Carry Look-ahead Adder (CLA) solves this problem by calculating the carry signals in advance, based on the input signals which results in reduced carry propagation time. The Propagate P and generate G in a full-adder, is given as:

Carry propagate Pi=Ai xor Bi

Carry generate Gi =Ai and Bi

III. Simulation Result

As shown in figure 4 Shows that the 16- bit booth multiplier. Figure 5 show that the simulation result of 16 bit multiplier output wave form. Table 1 indicate the comparatively analysis of 16 bit multiplier parameter like Delay, Speed, and power dissipation.

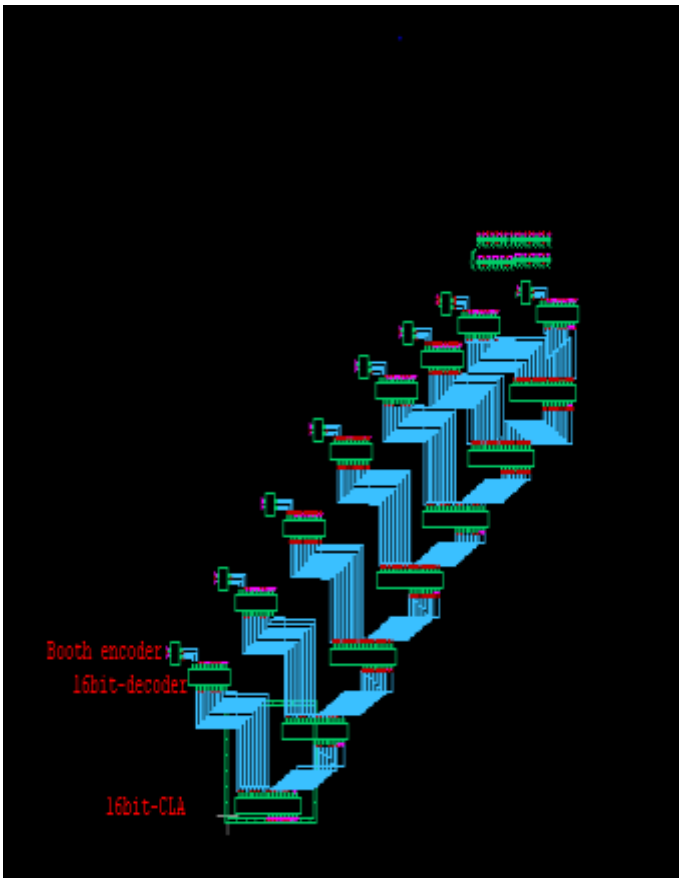
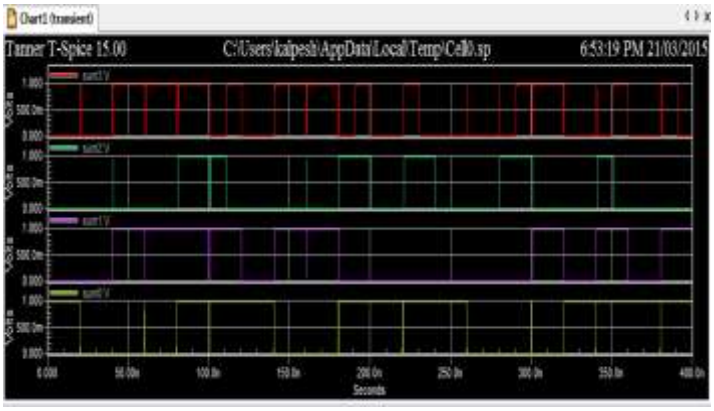
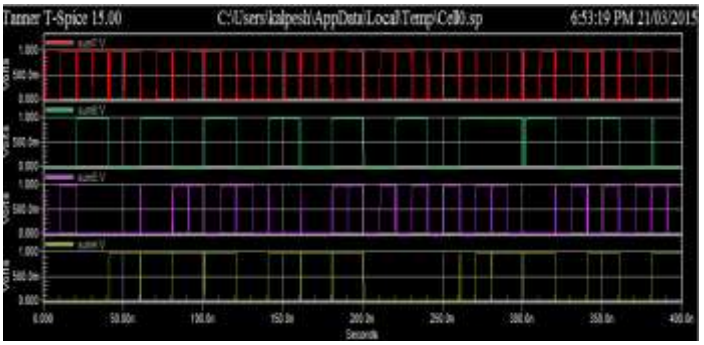
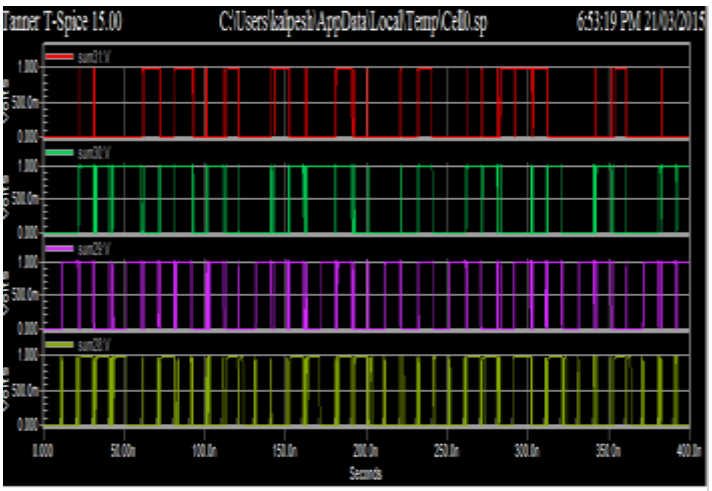


Figure 4: 16 bit multiplier







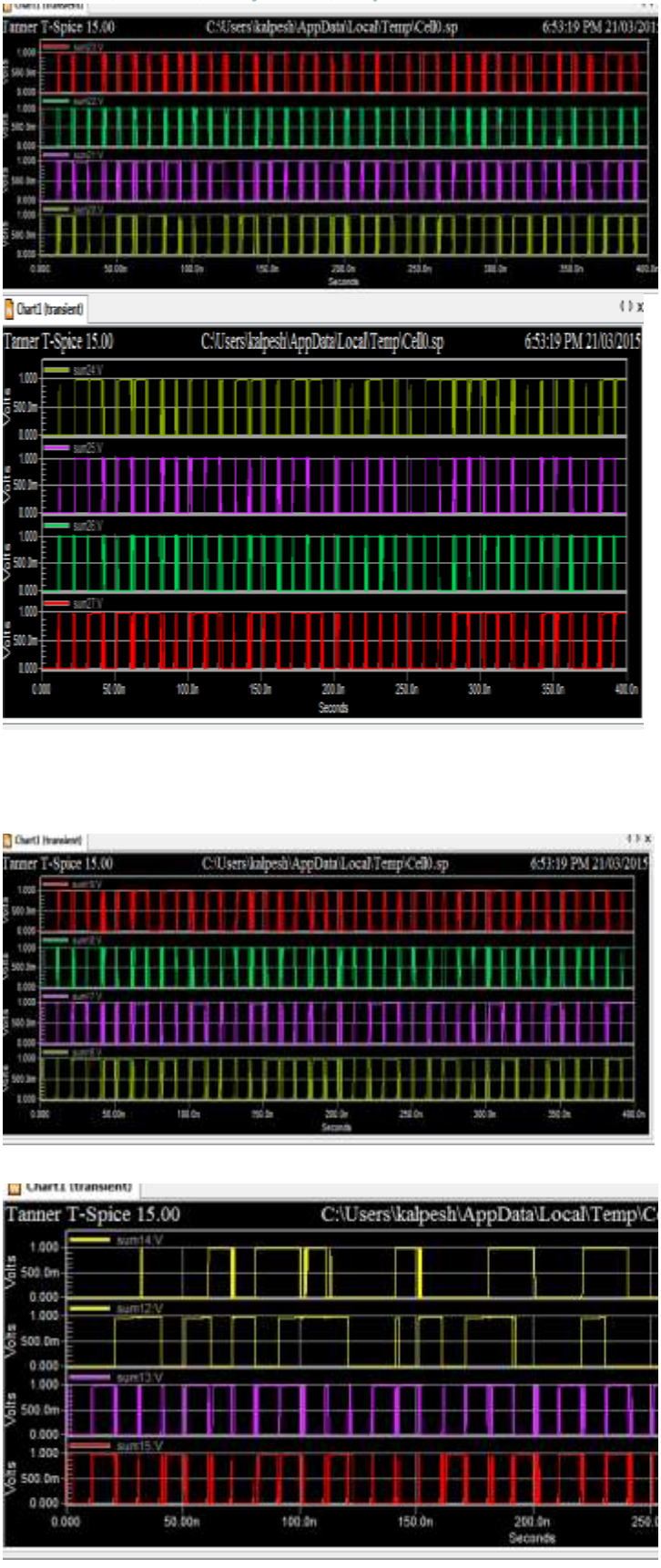


Figure 5: 16-bit Multiplier output waveform

Table 1: Comparative analysis of 16-bit Multiplier

Parameters	**GDI**	**CMOS**
Power dissipation	5.68mw	6.11mw
Delay	18.58mw	40.68mw

IV. CONCLUSION

From the simulation of 16-bit Multiplier one thing is clear that booth algorithm gives faster result comparatively. Mainly our goal is achieved by this method. As we can see that GDI is faster than conventional method but also improvement are available. We show that the number of transistors is reducing using GDI technique, also reduce the area and power dissipation as per requirement.

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