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PERFORMANCE ENHANCEMENT OF CARRY SPECULATIVE ADDER FOR LOW POWER VLSI

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Abstract-**Addition is one of the most commonly used arithmetic operation, which adds two operands and used to build advanced operations such as multiplication and division. They are generally used in applications such as arithmetic logic units and digital signal processors. The existing adders suffer from area overhead, critical path delay and power consumption. Low power is essential for portable multimedia devices employing various signal processing algorithms and architectures. Speculative adders are designed with variable latency that combines speculation technique in addition with correction methodology to attain high performance in terms of low area overhead. Carry Speculative Adder(CSPA) uses carry predictor circuit in order to reduce power consumption and computational time. It also uses error detection and error recovery circuit to detect the fault occured in the partial sum generator and to recover it to get accurate results. CSPA circuit produces error free output so that it can be used in many applications. This speculative adder can reduce the delay upto 11.89%.**

Keywords*:* Speculative adder ,variable latency, error detection, error correction

I. INTRODUCTION

In digital electronics, addition of binary numbers in different computers and other kinds of processors are performed using adders. Adder circuits are also used for calculating increment or decrement operations, addresses, table indices etc. They are used for many operations such as encoding, decoding, calculation etc., and have wide range of applications in many fields. The different formats like excess-3,gray code and Binary Coded Decimal(BCD) can be calculated using the adder circuits. The critical path is not often used in traditional adders, based on this analysis speculative adders have been designed. Traditional adders rely on its previous value for each output. In particular, the most significant bit(MSB) of the sum depends on the previous output bit, where n is the width of the block adder. As block adder width n increases, error growth will occur. This error grows proportionally with block adder width n. This error causes large area and large fanout in the circuit. Speculative adder can overcome the area problem but there occurs high error rate. For this error tolerance, variable latency adder[1] is designed along with the speculative adder. This variable latency adder contains error recognition and error correction circuit[2-3], which is used to overcome the high error rate. The overall design helps the speculative adder to employ in applications such as signal and image processing.

By choosing the developing concept in VLSI design, error tolerance (ET), a novel error tolerant adder (ETA I, ETA II, ETA III, ETA IV)is proposed in [4-5]. ETAI is classified into an accurate part and an inaccurate part to obtain approximate results. ETAI achieve enormous improvements in both speed performance and power consumption. ETAI is poor in the case of smaller inputs. ETAII cuts carry propagation to increase the speed of Addition. The performance of the adder for small input operands is considerably improved using ETAII, while the accuracy of ETAII for large input operands is degraded than ETAI. The degraded accuracy performance of ETA II for large input operands may restrict its usage. In ETAIII, the delay degrades and accuracy increases while power consumption improves. In ETAIV, the delay and accuracy increases, while area is high[5]. Variable latency designs may enhance the performance of those circuits in which the worst case delay paths are intermittently activated. The basic principle that gives the implementation of a variable latency resource is that of speeding up the process[6-7]. Variable latency units illustrate the property that the number of cycles taken to calculate their outputs varies depending on the input values.

Speculative technique is an optimization technique which is developed for improving the delay using prediction mechanism in arithmetic circuits. Static window addition (SWA), a specific function speculation technique for designing variable latency adders with high performance and low area overhead. A block, called a window, involves several consecutive input bits. Combining input bits into blocks, the carry chain length is compared to the block size with high probability. Variable Latency(VL) addition using static window adder (SWA) based speculative adders is faster than the Design Ware adder with area requirements for various adder

widths. A correlation aware speculative addition (CASA) is proposed in [11], which is a comprehensive lightweight extension to existing speculative adders which avoids the correlation between the most significant bit of the input operands and the carry in values to attain the accuracy of speculative adders[14]. It proves that CASA achieves a major reduction in error rate with small overhead in timing and area.

II. EXISTING TECHNIQUE

A . Carry Speculative Adder

Carry Speculative Adder (CSPA) is used to reduce the critical path delay of the circuit that rely on carry speculation is shown in Fig. 1. The n-bit CSPA is classified into several small block adders that are operated separately and carry predictor circuits. The size of each block adder is x-bit, except the leftmost block adder.

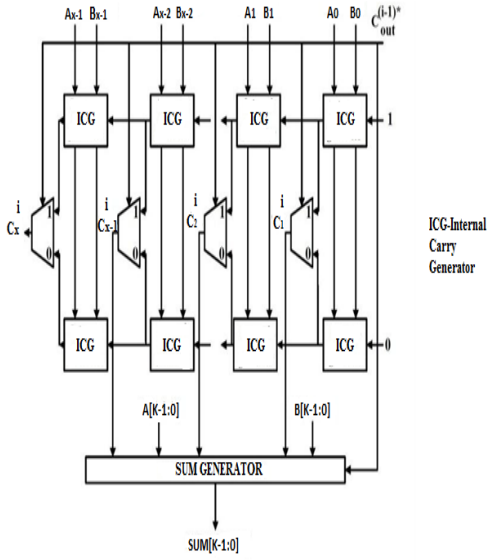

Fig. 1 Block Diagram for Carry Speculative Adder Unit

1. *Operation of CSPA*

When an input pattern is arrived, the internal carry generators and the carry predictor circuits operate parallely. The internal carry generator produces corresponding internal carry signals with respect to carry in signal "1" and "0". The carry predictor produces the predicted carryout bits of the block adders. The predicted carryout bit $(i-1)^{th}$ is given to the i^{th} block adder and is used as the select signal to the multibit multiplexer and the carry-in bit of the sum generator. Based on the multibit multiplexer select signal, the corresponding internal carry signals are selected and are given as inputs to the sum gum generator to produce a partial sum of the i^{th} block adder. The inputs to sum generator comes from the x bit input patterns, [x-2:0] bits from the multiplexor and $(i-1)^{th}$ carry predictor circuit. Since the carry predictor circuit uses input bit bear to Most Significant Bit(MSB), the results generated from the CSPA are almost correct.

B . Carry predictor

A carry predictor is used to predict the carryout bit of the corresponding block adder. To predict the carry-out bit of the corresponding block adder, carry predictor circuits uses the input bits that are near to MSB which reduces area and power consumption with minimal loss of accuracy. The probability of affecting the carry out bit is low when the input bits are near to Least Significant Bit (LSB) are used. Hence, a low error rate can be maintained, if the carry predictor circuit only uses the input bits near the MSB to predict the carryout bit, and the area overhead of the carry predictor circuits can be reduced. Since the probability of a carryout bit of the block adder depends on the k previous bit positions is 1/2k because the probability of propagate signal Pi (ai XOR bi) having a value of 1 is 1/2 in each bit position.

C . Carry Generator and Sum Generator

In Traditional Full Adder, the carry bit is produced after three gate delays. A Modified Full Adder (MFA) is used in block adder of the CSPA to separate carry generator and sum generator. The MFA uses an additional logic gate compared to Traditional Full Adder (TFA), to reduce the delay of the carry bit which

produces after two gate delays with higher power consumption. CSPA is implemented using two carry generators and a sum generator in block adders to reduce power consumption.

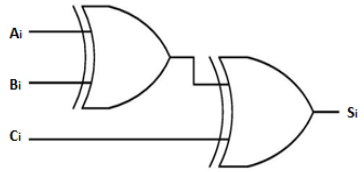

Fig. 2 Block Diagram of Sum Generator

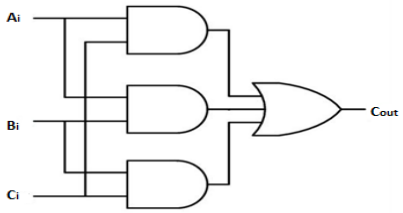

Fig. 3 Block Diagram of Carry Generator

D . Speculative Addition

Speculative addition has been firstly used in the context of asynchronous design. A fast asynchronous k-bit speculative adder is extended with different abort detection networks, each associated with a different delay condition occurring in the addition circuit. It involves a two-cycle operation. The addition is started in the first cycle, and the result is assumed to be correct. A parallel carry propagation network checks whether or not the operation has long carry paths. Should this be the case, the system stalls for the duration of an additional clock cycle where the original addition operation has sufficient time to complete. Some bypass logic is required to allow the sum to be generated using these early carries. The detection of long carry chains takes place only in the second cycle, so the previous result may need to be overwritten.

Propagate/Generate (P/G) signals for single digits or for groups of digits represents the carry propagation (the output carry for those digits is equal to the input carry) and carry generation (the sum of those digits always produces an output carry independent of previous carries). Notice that the critical path of the architecture depends on the error condition, which is a global signal, and still requires an O(log n) time complexity.

The advantage of using CSPA is that it requires less circuitry than carry select using only 2/3 as many half-precision adders and no multiplexer. It also can use less power.

III. PROPOSED TECHNIQUE

A . Modified Carry Speculative Adder

High speed adders depend on well-established parallel-prefix architectures such as Brent-Kung, Kogge-Stone, Sklansky, Han-Carlson, Ladner-Fischer, and Knowles. These architectures operate with fixed latency. Better performance can be achieved by using variable latency adders is shown in Fig. 4.

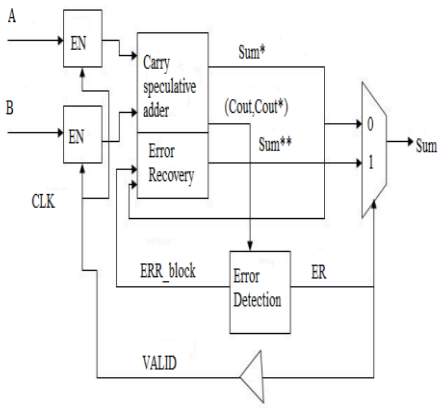

Fig. 4 Block Diagram of Carry Speculative Adder with Variable Latency

1 . Stages in Han-Carlson Adder

There are mainly three computational stages in Han Carlson Adder. They are

- Preprocessing
- Speculative Prefix Processing
- Post Processing

Preprocessing

In the pre-processing stage the generate gi and propagate pi signals are computed as

gi=ai bi

pi=ai^bi

Speculative Prefix-Processing

The speculative prefix-processing stage is one of the main differences compared with the standard prefix adders recalled in previous section. Instead of computing all g[i:0]and p[i:0], only a subset of block generate and propagate signals is calculated; in the post processing stage approximate carry values are obtained from this subset. The output of the speculative prefix-processing stage will also be used in the error detection and in the error correction stages.

In general, the calculated propagate and generate signals for the speculative Han-Carlson architecture are:

(g,p)[i:0] for: i<=k

(g,p)[i:i-k+1] for: i>k,i odd

(g,p)[i:i-k] for: i<k, I even

Post Processing Stage

In the post-processing stage we firstly compute the approximate carries, ci , and then use them to obtain the approximate sum bits si as follows:

si=pi^ci

B . Variable Latency Adders

A variable latency adder uses speculation: the exact arithmetic function is replaced with an approximated function that is faster and gives the correct result most of the time, but not always. The approximated adder is augmented with an error detection network that asserts an output signal when speculation fails. In this case (misprediction),another clock cycle is needed to attain the correct result with the help of a correction stage. A novel variable latency speculative adder based on Han-Carlson parallel prefix topology uses number of stages while requiring a reduced number of cells and simplified wiring.

C . Error Detection and Recovery

In CSPA, the addition operation is based on speculation which may produce accurate or inaccurate results. An error detection circuit is used to check whether produced results are accurate or inaccurate. The Error Recovery Circuit corrects the incorrect partial sum bits of the block adders according to the Err_block signal.

IV. SIMULATION RESULTS

A. Error Detection

Simulation output for the Error Detection Circuit is shown in Fig. 5 er signal is error signal if it is 1, it indicate the occurrence of error otherwise it denotes no error.

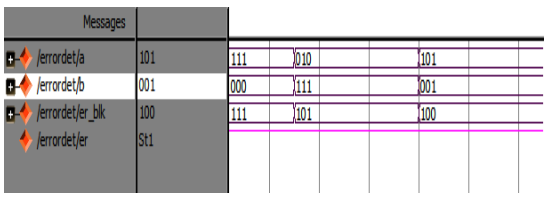

Fig. 5 Simulation result for error detection circuit

B. Error Recovery

Simulation output for the Error Recovery Circuit is shown in Fig. 6 if the er signal is 1 the error is rectified and the correct sum is generated.

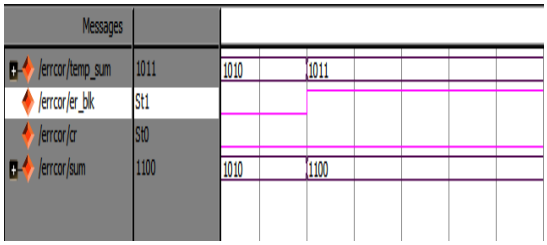

Fig. 6 Simulation result for error recovery circuit

C. Han Carlson adder

Simulation output for Han Carlson topology is shown in Fig. 7 with propagate and generate signals.

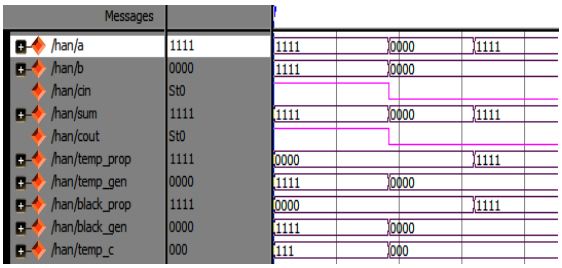

Fig. 7 Simulation result for han Carlson adder

D. Modified Carry speculative adder

Simulation output for the 16-bit CSPA is shown in Fig. 8. The input 16 bit a and b along with the carry in bit cin is fed to the CSPA with contain the adder block, predictor block, error detection and error correction block. P_sum is the final sum output produced by the CSPA.

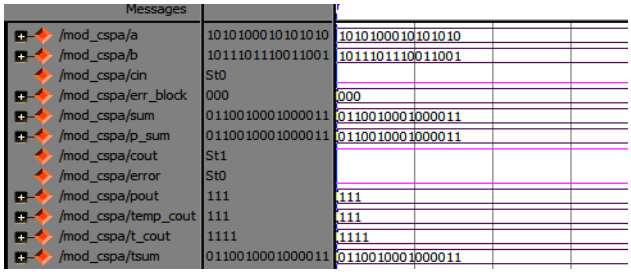

Fig. 8 Simulation result for 16-bit CSPA

E. Carry predictor circuit

Simulation output for carry predictor circuit is shown in Fig. 9.

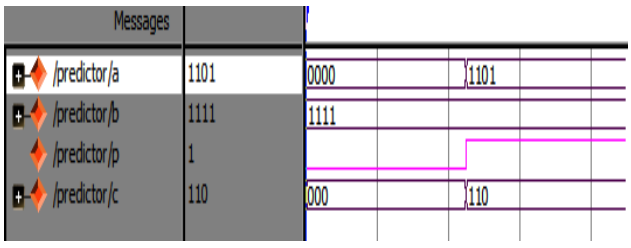

Fig. 9 Simulation result for predictor circuit

Table. 1 Comparison of SCSA and CSPA

ADDER TYPE	TOTAL no.OF GATES USED	DELAY (ns)	POWER (mW)
SCSA (16 BIT)	654	26.725	112
CSPA (16 BIT)	502	18.259	89
MODIFIED CSPA-16 BIT	342	16.599	72

Table 1 shows the comparison of SCSA and the proposed CSPA. This clearly defines that the proposed CSPA has low power consumption and low delay.

V. CONCLUSION

A Variable latency adder that combines the speculative adder with error detection and error correction unsigned random inputs called variable latency carry speculative adder. The sum and carry generator are isolated in CSPA so that the carry signal and the partial sum bit can be calculated faster. Carry predictor circuit of the block adder only allows the input bit nearer to the MSB to predict the carryout bit. The above discussed error detection circuit indicates the block adder which produce an incorrect carry-out bit and the error recovery circuit focuses on correcting the block adders with incorrect partial sum bits. Based on the comparison of CSPA and SCSA,CSPA reduces delay upto 11.88% and computational complexity upto 11.39%.

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