



DESIGNING A HIGH SPEED LOW POWER OF TWO STAGE DYNAMIC COMPARATOR

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Abstract- Designing a high speed, low power of two stage dynamic comparator is presented. Low power consumption is a great interest because it increases the battery lifetime. The main block in many applications is the analogue to digital converter (ADC) which serves as an interface between the analog world and a digital processing unit. In this circuit the first stage of the preamplifier stage is limited to $v_{dd}/2$ and NMOS is connected at the second stage for reducing power consumption. The second stage of the comparator is to start comparison based on inputs and reference voltages. Simulation results prove that the proposed comparator speed ups the conventional comparator and also reduces power. Furthermore, proposed comparator is followed by post layout. This method will be designed and its power is evaluated in the ASIC design GUI software of 130 nm technology.

Keywords- Analog to Digital Converter (ADC), Application Specific Integrated Circuits (ASIC), Graphic User Interface (GUI).

I. INTRODUCTION

Low power and high speed are natural candidates for portable electronic devices. Comparators are crucial circuits in analogue-to-digital converters (ADCs) to convert analogue signals into digital form. The comparator is a device used to sense when an arbitrary varying signal reaches some threshold level. A comparator is designed to give limited output voltages that easily interface with digital logic. The accuracy of comparators depends on voltage gain, common-mode rejection ratio (CMRR), input offset voltage. There is a demand for portable devices, the main thrust is lower methods for high speed applications. Power can be reduced by choosing smaller size process. Comparators play a main role for high speed and low power. Pre amplifier Comparators are suffering from more offset voltages. Whereas, dynamic comparator will make comparison for every clock cycle and require less offset voltages.

Comparators are important role in efficiency of commonly used ADCs, such as Flash and SAR ADCs [1–15]. Generally, moving toward the smaller feature size allows for the reduction in the power consumption and higher speed. However, the process variation and mismatch increases at finer processes and limits the performance of the ADCs. One of the critical parts of an ADC greatly influenced by the process variation and mismatch is the comparator. Static comparators have been used in the past, however, they are impractical for portable applications because of their limited speed and significant amounts of power consumption [1]. One-stage dynamic comparators were proposed to reduce the power consumption and improve speed [2]. These comparators, however, suffer from an inherent trade-off between the power consumption and offset voltage. Moreover, one-stage dynamic comparators suffer from kick-back noise caused through the capacitive path from the output nodes to the input nodes of the comparator [3]. Two-stage dynamic comparators are proposed to mitigate the kickback noise and it will decouple the offset versus speed trade-off of the single-stage dynamic comparators [4]. Comparators are proposing a low-power, high-precision dynamic comparator with a novel time-

domain bulk-tuned offset cancellation is used as optimized to minimize the noise and offset. OC schemes are proposed which samples the offset and closed loop bulk timing will be cancelled. It consumes negligible power, does not sacrifice speed, or require complex timing control [5]. In order to break the deadlock between the offset and the power consumption at low power and the low offset dynamic comparator are proposed. The double phase architecture takes the advantage of a cascade of amplifying stage and a usual latch stage. The structure benefits from two phases signaling to cancel the mismatch of the inner devices. The offset voltage was obtained using analytical derivations as a function of mismatch and delay [6]. Comparators are proposed as single-stage dynamic comparator with a large input common-mode range. It is compared with dynamic comparators along with their size input transistors and load capacitance. Comparators power are reduced [7].

Calibration technique will embrace comparator decision time in order to calibrate gain errors and capacitor mismatches in pipelined analog to digital converters (ADC). Proposed techniques improve the signal-to-noise-and distortion ratio. Capacitor (DAC) proposed that will have an effecting reference voltage and accurate voltage division is provided [8-13]. Comparator are proposed to reduce the power consumed in the pre-amplifier stage by preventing the operation of the pre-amplifier stage when the output differential voltage of the latch stage is large enough. Then, the proposed technique was employed in these circuits and the average power consumption, including the XOR gate at the same clock frequency was measured. Thus reduces the power consumption of dynamic comparator [14]. A high speed, low power comparator is achieved by minimizing voltage variation of the first stage with an acceptable offset voltage latch stage is activated more than conventional circuit by improving input common mode range [15].

II. CONVENTIONAL COMPARATOR

Conventional of two-stage dynamic comparator is shown in Fig.1. This comparator is composed of two stages: the preamplifier stage (first stage) and the latch stage (second stage). Pre-amplifier amplifies the signal and the latch will compares signal. The operation of this circuit is described as follows.

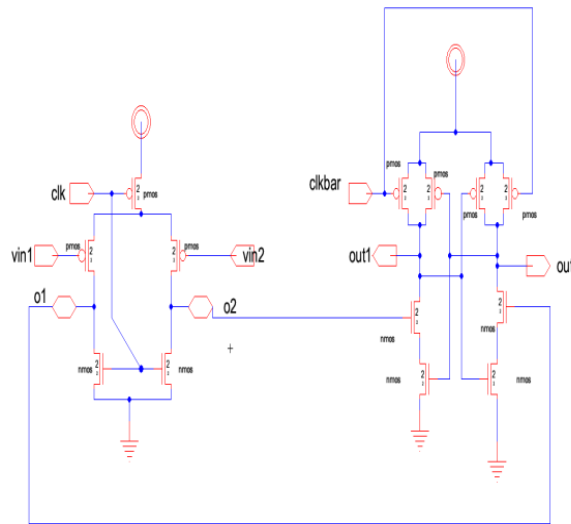


Fig. 1 Preamplifier and latch stages of the conventional two-stage dynamic comparator

Before the comparison is made, the comparator state is reset ($\text{clk} = "1"$, $\text{clkbar} = "0"$) to discharge the output nodes of the first stage to Gnd and charge the output nodes of the second stage to Vdd. In the next phase, the evaluation phase, " clk " and " clkbar " goes to " 0 " and " 1 ", respectively, to start the comparison. Then, the output voltages of

The first stage ($V_{o1+} - V_{o2}$) start to grow gradually. The growth rate depends on the magnitude of the input differential voltage ($V_{in1} - V_{in2}$). Gradually, a differential voltage appears at the output nodes of the first stage

(i.e., $V_{o1} - V_{o2}$). When the output voltages of the first stage approach the threshold voltage of an NMOS transistor (M10, M11), the second stage (latch) is activated.

Hence, the positive feedback nature of the latch amplifies the differential voltage until the latch is locked. Consequently, the voltage of one of the output nodes of the latch stage settles at Gnd and the other one settles at Vdd while the output voltages of the first stage both reach Vdd. Thus the output nodes of the first stage are discharge to the ground during the reset phase and charged toward Vdd during the evaluation phase. The output nodes of first stage reaches gnd and output nodes of second stage reaches vdd. The power is calculated for conventional comparator 6.33567 MW. As a result this makes the conventional comparator is an unsuitable choice for low power, high resolution application.

III. PROPOSED COMPARATOR

The proposed comparator is shown in Fig.2. At the reset phase, the node voltages of the first stage are discharged to V ($V_{dd}/2$) which is large to keep the second stage active. To avoid a DC power consumption in the second stage, NMOS is placed to cut the path from Vdd to Gnd during the reset phase.

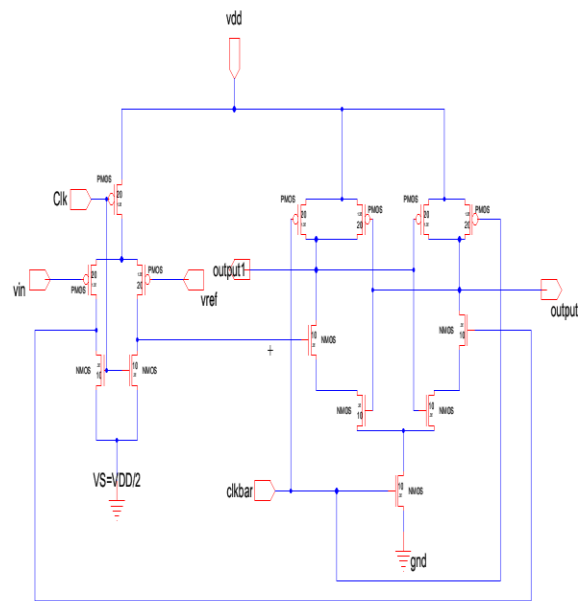


Fig. 2 Proposed two stage dynamic comparator and its difference in comparison to the conventional comparator.

The voltage of the first stage of the comparator is limited to $v_{dd}/2$. The power consumption of the first stage of the comparator is a dominant part of total power consumption is reduced by a factor of two when compared to the conventional comparator. In order to activate the latch stage the proposed method has no delay time to charge the output voltage of the first stage. Due to the large common mode voltage at input of the latch ($>v_{dd}/2$) enhance the speed of the latch. At the beginning of evaluation phase the first stage of output voltage is large enough to activate the second stage. This strong activation enhances the speed of the latch. While decreasing clock time period the proposed method operates at high speed, because of frequency increases. So, thus pre-amplifier and latch stage enhance the speed while compare to conventional comparator.

The size of the input transistor of the two stages should be designed carefully. By adding an nMOS at the latch stage reduces the power consumption. Thus the proposed comparator improves speed and reduces the power consumption.

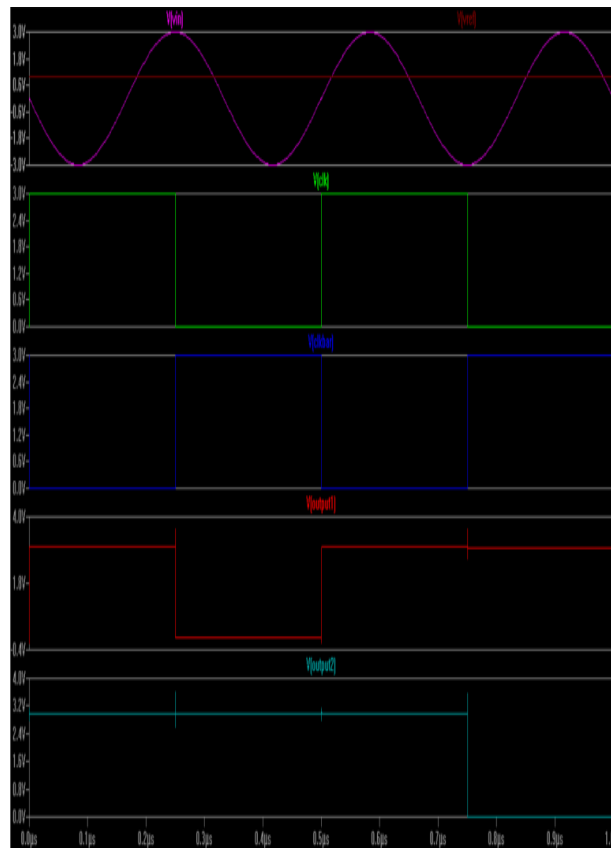


Fig. 3 Simulation result of 2MHZ

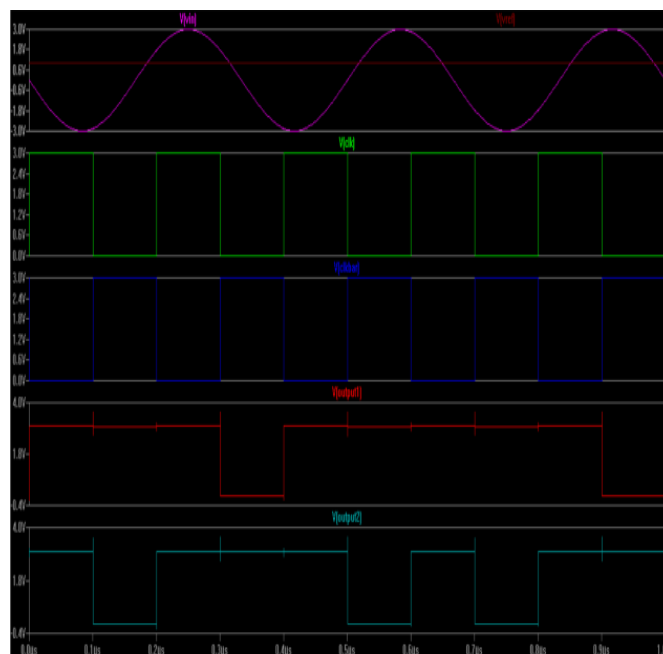


Fig. 4 Simulation result of 6MHZ

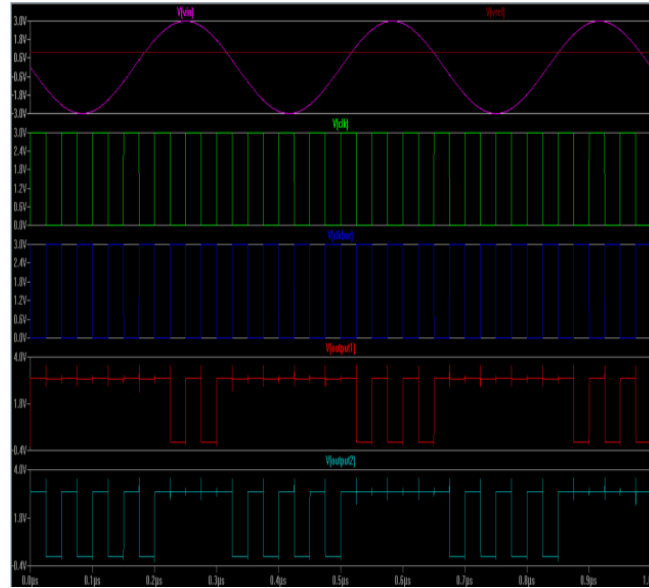


Fig. 5 simulation result of 20MHZ

IV. SIMULATION RESULTS

Comparators are also known as mixed-mode circuits (analog-digital). Their specification depends upon the technology, which is used. To draw fair comparison the proposed circuits are carefully designed in 130 nm CMOS technology. The circuits are designed as similar 2.5mV input transferred offset voltage and 420 Uw power consumption at 500 MHZ clock frequency except for the circuit [10]. These circuits consume a significant amount of power that is not adjustable. These figures show that the proposed comparator is faster than the conventional comparator with a factor of two.

Fig.3 represents the speed of the circuits. When $v_{in} > v_{ref}$ the circuits starts comparison and result as output1 settles at gnd and output 2 settles at vdd. When $v_{in} < v_{ref}$ the output 1 settles at vdd and output 2 settles at gnd. While giving clock period of 250n to 500n the proposed comparator operates at good speed. Fig.4 operates at 6MHZ. The clock period ranges from 100n to 200n it increases the frequency and operates at maximum speed. Fig.5 operates at 20MHZ. Here the clock period ranges from 25n to 50n the proposed comparator works at high speed. On decreasing the clock period, frequency get increases and thus proposed comparator operates at high speed. Moreover, the proposed comparator works on wider input common mode ranges, since the latch stage is activated faster when compared with other methods.

$$F = 1/T$$

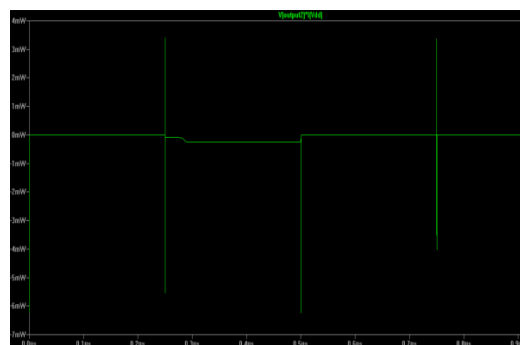


Fig. 6 Power analysis of 2MHZ

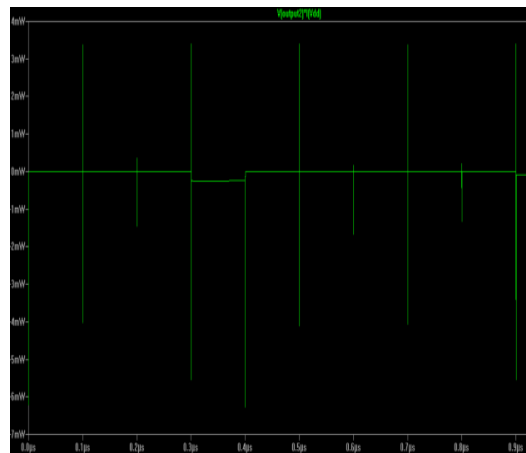


Fig.7 Power analysis of 6MHZ

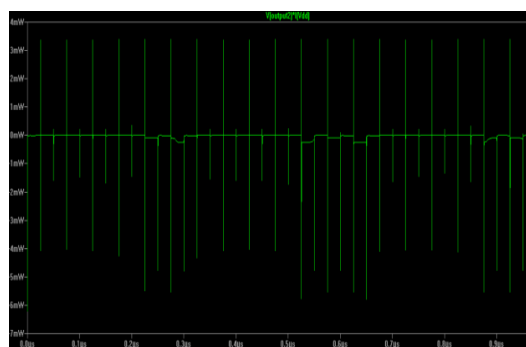


Fig. 8 Power analysis of 20MHZ

Simulation result of power for the proposed comparator is shown above. Fig.6 shows that power is measured as 5.9197MW. Fig.7 shows that power is measured as 4.56636 MW. Fig.8 shows that power is measured as 4.38733 MW. Thus, different power is measured by comparing these while giving clock period low, power is reduced. On inserting nMOS at the second stage of latch in order to reduce power consumption. Through using proposed circuit suggest best clock frequency and an acceptable power consumption.

V. POST LAYOUT SIMULATION

Post layout simulation are performed should be compared with schematic results. Fig. 9 shows post layout simulation along with schematic simulation results. Fortunately, the symmetry of the layout, post layout simulation results almost matches schematic results.

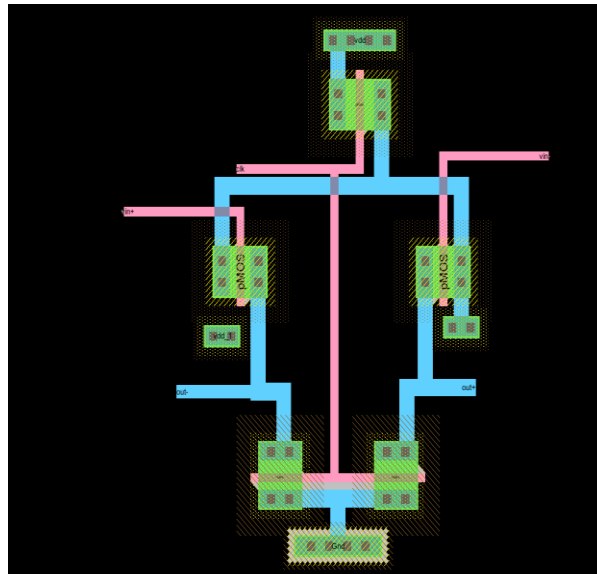


Fig.9 Post layout of preamplifier

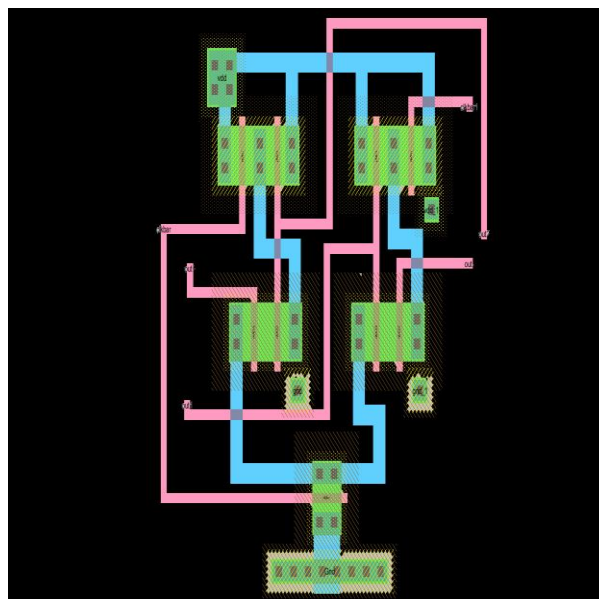


Fig. 10 Post layout of dynamic latch

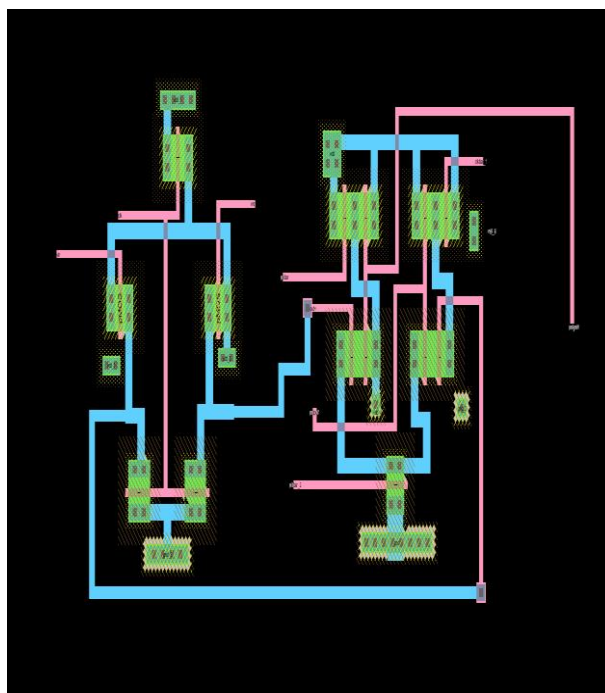


Fig. 11 Post layout of proposed comparator

The proposed circuit represents a high speed comparator with acceptable amount of power consumption. By using proposed circuit, the maximum clock frequency 20 MHZ is achieved. Fig.12 shows transient analysis of post layout it is similar to schematic results. Fig. 13 shows power measurement of post layout same results as a schematic.

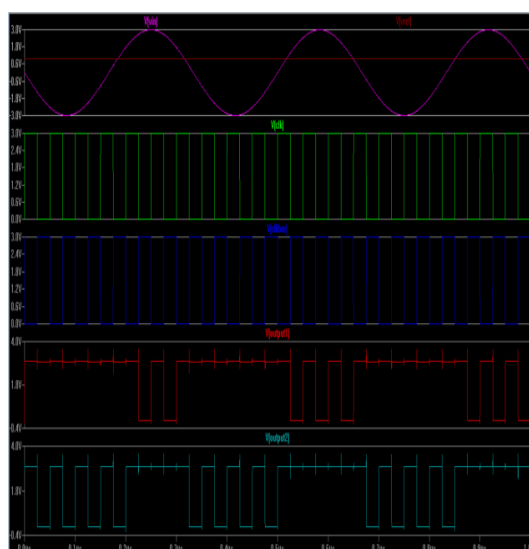


Fig. 12 Simulation of post layout

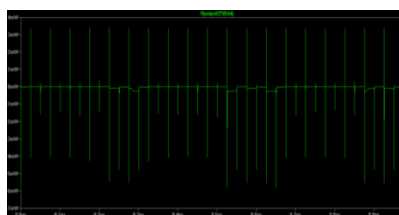


Fig. 13 Power of post layout

VI. CONCLUSION

Designed a high speed, low power comparator is presented. In this circuit, the voltage variation of the first stage is limited to $v_{dd}/2$ and NMOS is connected at the second stage for reducing power consumption. Moreover, the speed of the circuit and the input common mode is increased. The post layout simulation proves similar to the schematic results. As a result, the proposed comparator is efficient for high speed, low power applications. These comparators are used in analog to digital converter (ADC) applications like flash ADC, successive approximation register ADC.

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