



## DESIGN AND ANALYSIS OF VEDIC MULTIPLIER BASED ON YAVADUNAM TAVADUNIKRITYA VARGA YOJAYET SUTRA

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**ABSTRACT:** In the modern world of digitization, processing of data in real time requires an increase in the operating speed of a system. The use of Vedic mathematics lies in the formula that reduces the typical calculation in the conventional mathematics to very simple one. This paper deals with the design of Vedic multiplier using “Yavadunam Tavadunikritya Varga Yojayet” of ancient Indian Vedic mathematics. The Unique architecture is designed for “Yavadunam Tavadunikritya Varga Yojayet” sutra. Which uses the multipliers and a comparison of the power, delay and area constraints are obtained using Xilinx Spartans 3E which using the Wallace tree multiplier in the proposed method power and delay are significantly low compared to the other multipliers such as array and Baugh-Wooley multiplier.

**Key Words:** Vedic mathematics, “Yavadunam Tavadunikritya Varga Yojayet”, Wallace tree multiplier, Baugh-Wooley multiplier.

### I. INTRODUCTION

Multipliers are key components of many high performance systems such as microprocessors, DSP, various FIR filters, etc. [3]. A performance of a system is generally determined by the performance of the multiplier, because the multiplier is generally the slowest element [5]. The need of high speed multiplier is increasing as the need of high speed processors is increasing. The speed of multipliers determines the efficiency of such a system. In any system design, the three main constraints which determine the performance of the system are speed, area and power requirement [1]. Multiplication is an operation of multiply one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT) [11].

The Vedic multiplier plays an important role in increase the processing speed. The multipliers are capable of multiplying any number of bits based on their architecture [6]. The word Veda means “knowledge” and Vedanta means the ultimate end of knowledge [8]. The term ‘Veda’ means storehouse of knowledge. Vedic mathematics is reconstructed from the ancient Indian scriptures (Vedas) by “Swami Bharati Krishna Tirthaji Maharaja (1884-1960) after his eight years of research on vendors. Vedic mathematics is an ancient form of mathematics. It is based on 16 sutras and 13 sub sutras which transact different branches of mathematics like algebra, geometry and arithmetic.

These sutras describe the way that the mind naturally works and are therefore a great help in directing the student to the appropriate method of solution. This work focuses on “Yavadunam Tavadunikritya Varga Yojayet” in Vedic mathematics. The 16 sutras and 13 sub sutras of Vedic mathematics are given in the Table I and Table II.

This sutra can be applied to obtain squares of numbers closer to base value. The hardware architecture of the Vedic multiplier is presented and is shown to be very similar to that of the popular array multiplier [9]. In this paper, proposed Vedic multiplier using “Yavadunam Tavadunikritya Varga Yojayet” Vedic mathematics is implemented with Verilog HDL language.

Table I: Vedic sutras

| Sl. No | Sutras                         | Meaning                                                                                     |
|--------|--------------------------------|---------------------------------------------------------------------------------------------|
| 1      | Ekadhikena Purvena             | One more than the previous one                                                              |
| 2      | Nikhilam Navatascarama Dasatah | All from 9 and last from 10                                                                 |
| 3      | Urdhva - Tiryagbhyam           | Criss-cross (Vertically and cross-wise)                                                     |
| 4      | Paravartya Yojayet             | Transpose and adjust (Transpose and apply)                                                  |
| 5      | Sunyam Samyasamuccaye          | When the samuchchaya is the same, the samuchchaya is zero, i.e it should be equated to zero |
| 6      | (Anurupye) Sunyamanyat         | If one is in ratio, the other one is zero                                                   |
| 7      | Sankalana - Vyavakalanabhyam   | By addition and by subtraction                                                              |
| 8      | Puranapuranaabhyam             | By the completion or non-completion                                                         |
| 9      | Calana Kalanabhyam             | By Calculus                                                                                 |
| 10     | Yavadunam                      | By the deficiency                                                                           |
| 11     | Vyastisamastih                 | Specific and General (Use the average)                                                      |
| 12     | Sesanyankena Caramena          | The remainders by the last digit                                                            |
| 13     | Sopantyadvayamantyam           | The ultimate & twice the penultimate                                                        |
| 14     | Ekanyunena Purvena             | By one less than the previous one                                                           |
| 15     | Gunitasamuccayah               | The product of the sum of coefficients in the factors<br>(The whole product)                |
| 16     | Gunakasamuccayah               | Set of Multipliers                                                                          |

Table II: Vedic sub sutras

| Sl. No | Sub Sutras                               | Meaning                                                                                                                    |
|--------|------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|
| 1      | Anurupyena                               | Proportionately                                                                                                            |
| 2      | Sisyate Sesamjnah                        | The remainder remains constant                                                                                             |
| 3      | Adyamadyenantyamantyena                  | The first by the first and last by the last                                                                                |
| 4      | Kevalaih Saptakam Gunyat                 | In case of 7 our multiplicand should be 143                                                                                |
| 5      | Vestanam                                 | By osculation                                                                                                              |
| 6      | Yavadunam Tavadunam                      | Lessen by the Deficiency                                                                                                   |
| 7      | Yavadunam Tavadunikrtya Varganca Yojayet | Whatever the extent of its deficiency, lessen it still to that very extent; and also set up the square of that deficiency. |
| 8      | Antyayordasake                           | Whose last digits together total 10 and whose previous part is exactly the same                                            |
| 9      | Antyayoreva                              | Only the last terms                                                                                                        |
| 10     | Aamuccayagunitah                         | The sum of the coefficients in the product                                                                                 |
| 11     | Lopanasthapanabhyam                      | By alternate elimination and retention                                                                                     |
| 12     | Vilokanam                                | By observation                                                                                                             |
| 13     | Gunitasmuccayah Samuccayagunitah         | The product of sum of the coefficients in the factors is equal to the sum of the Coefficients in the product.              |

## II. EXISTING METHOD USING ARRAY MULITPLIER

In existing method, the squaring is carried out by using the array multiplier along with the 2's complement and the adder unit. Array multiplier circuits are based on add and shift algorithm. An array multiplier is a digital combinational circuit that is used for the multiplication of two binary numbers by employing an array of full adders and half adder. This array is used for nearly product terms involved.

|    |      |      |      |      |      |      |      |
|----|------|------|------|------|------|------|------|
|    |      |      |      | a3   | a2   | a1   | a0   |
|    |      |      |      | b3   | b2   | b1   | b0   |
|    |      |      |      | a3b0 | a2b0 | a1b0 | a0b0 |
|    |      |      | a3b1 | a2b2 | a1b1 | a0b1 |      |
|    |      | a3b2 | a2b2 | a1b2 | a0b2 |      |      |
|    | a3b3 | a3b2 | a3b1 | a3b0 |      |      |      |
| p7 | p6   | p5   | p4   | p3   | p2   | p1   | p0   |

Fig. 1: 4×4 Array Multiplier

The main disadvantage of array multiplier is that the worst case delay of the multiplier is proportional to the width of the multiplier and the speed will be very low for the wide multiplier. The power consumption is also the major drawback with this type of multiplier usage. Even though, it is easily scalable and pipelined and also it is easy to place and route.

## III. YAVADUNAM TAVADUNIKRITYA VARGA YOJAYET

The meaning of the sutra is whatever the deficiency subtracts that deficit from the number and write alongside the square of the deficit. The sutra is used as Shortcut to square a number in Vedic Mathematics. Yavadunam Tavadunikritya Varga Yojayet is the corollary (sub sutra) to Sankalana – Vyavakalanabhyam, the seventh sutra of Vedic mathematics.

This sutra is used for simultaneous equations wherein the equations are added and subtracted. This results in two new equations which are simpler and can be solved easily than the conventional method. It can be used for larger coefficients also.

### Algorithms:

**Algorithm 1:** If the numbers are near and less than the basis of 10.

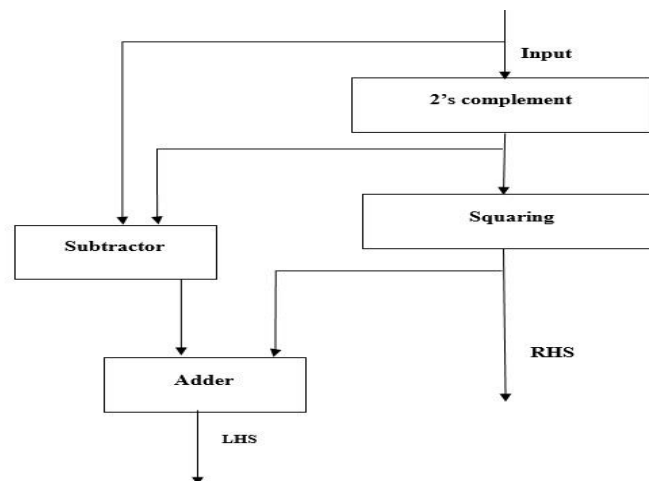


Fig. 2: Architecture of Less than base number

**Example:  $996^2$**

Subtract the number from the nearest power of 10.

$$1000-996=4$$

Subtract this deficit from the number:  $996-4=992$

Since, the nearest power of ten is 1000, add three zeros to this result: 992,000

Square the deficit:  $4 \times 4 = 1$

Add this to 992,000 to get the answer

$$996^2 = 992,016.$$

**Algorithm 2:** If the numbers are near and greater than the basis of 10.

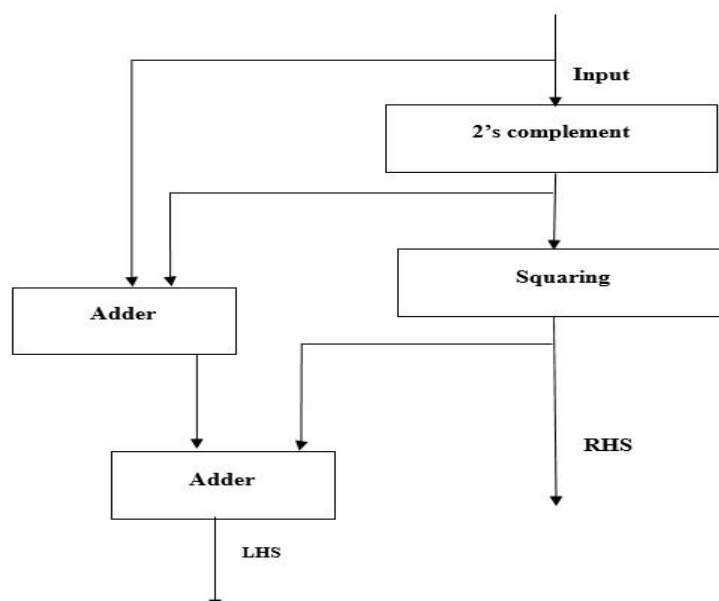


Fig. 3: Architecture of greater than base number

**Example:  $10025^2$**

Subtract the nearest power of 10 from the number.

$$10025-10000=25$$

Add this surplus to the number:  $10025+25=10050$

Since, the nearest power of ten is 10000, add four zeros to this result: 100,500,000

Square the surplus:  $25 \times 25 = 625$

Add this to 100,500,000 to get the answer

$$10025^2 = 100,500,625.$$

**Algorithm 3:** If the numbers are near to the multiplies of 10, 100, 1000, --- for this we combine the upa-sutra “Anurupyena” and “Yavadunam Tavadunikritya Varga Yojayet” together.

#### IV. PROPOSED METHOD OF VEDIC MULTIPLIER

In this proposed method, Vedic multiplication is performed by using the different multipliers such as, Wallace tree multiplier and Baugh Wooley multiplier.

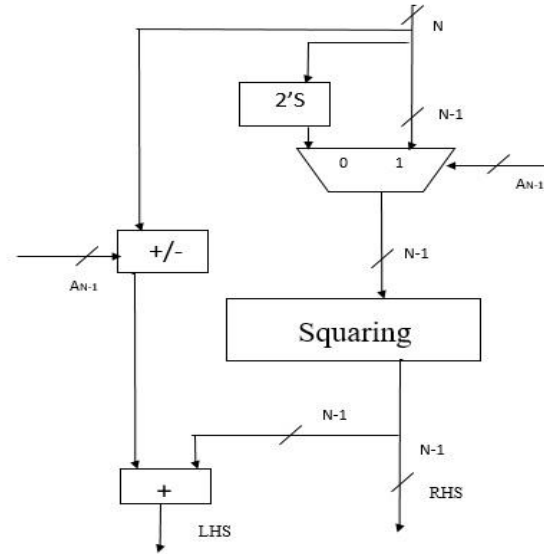


Fig. 4: Proposed architecture of Vedic multiplier

#### A. Wallace tree multiplier:

A Wallace tree multiplier is an efficient hardware implementation of a digital circuit that multiplies two integers. There are three important steps in Wallace tree multiplier. One advantage of the Wallace tree is it has small delay. The main disadvantage of Wallace tree is complex to layout and has irregular wires.

#### B. Baugh Wooley multiplier:

The Baugh-Wooley algorithm is a well-known iterative algorithm for performing multiplication in digital signal processing (DSP) applications. Decomposition logic is used by the Baugh - Wooley algorithm to enhance the speed and to reduce the critical path delay. The Baugh-Wooley multiplier using decomposition logic is presented here, which increases speed when compared to Booth multiplier.

The design of 4\*4 Vedic multiplier is used as a block for the multipliers [1]. Here Vedic multiplier is implemented by using two Vedic mathematics sutras. I.e. “Anurupyena” and “Yavadunam Tavadunikritya Varga Yojayet”. The architecture of Vedic multiplier contains 4 blocks of equal size. I. e. Each block consists of 4\*4 inputs are partitioned according to “Yavadunam Tavadunikritya Varga Yojayet” sutra.

## V. RESULTS

The Vedic algorithm is synthesized using 6v1x760ff1760-2 device in Xilinx Virtex 3E family [2]. The synthesis results, device utilization summary and time delay for Vedic, array, Wallace and Baugh -Wooley multipliers are presented in Table III.

| Messages |          |          |          |          |  |  |  |
|----------|----------|----------|----------|----------|--|--|--|
| + /sq/b  | 1111     | 1101     | 1111     | 1001     |  |  |  |
| + /sq/o  | 11100001 | 10101001 | 11100001 | 01010001 |  |  |  |
| + /sq/t  | 0001     | 0011     | 0001     | 0111     |  |  |  |
| + /sq/s  | 1110     | 1010     | 1110     | 0010     |  |  |  |
| + /sq/a  | 1110     | 1010     | 1110     | 0101     |  |  |  |
| + /sq/u  | 00000001 | 00001001 | 00000001 | 00110001 |  |  |  |
| + /sq/r  | 0001     | 1001     | 0001     | 0001     |  |  |  |
| + /sq/l  | 0000     | 0000     |          | 0011     |  |  |  |

Fig. 5: Simulation results for Vedic multiplier using Array multiplier

| Messages |           |          |          |          |  |
|----------|-----------|----------|----------|----------|--|
| /sq/b    | -No Data- | 1101     | 1010     | 0011     |  |
| /sq/o    | -No Data- | 10101001 | 01100100 | 00001001 |  |
| /sq/t    | -No Data- | 0011     | 0110     | 1101     |  |
| /sq/s    | -No Data- | 1010     | 0100     | 0110     |  |
| /sq/a    | -No Data- | 1010     | 0110     | 0000     |  |
| /sq/u    | -No Data- | 00001001 | 00100100 | 10101001 |  |
| /sq/r    | -No Data- | 1001     | 0100     | 1001     |  |
| /sq/l    | -No Data- | 0000     | 0010     | 1010     |  |

Fig. 6: Simulation results for Vedic multiplier using Wallace tree multiplier

| Messages |                  |                  |  |  |  |  |  |                  |  |
|----------|------------------|------------------|--|--|--|--|--|------------------|--|
| /dmul/a  | 1100             | 1110             |  |  |  |  |  | 0111             |  |
| /dmul/b  | 1100             | 1101             |  |  |  |  |  | 0111             |  |
| /dmul/d  | 100000           | 100000           |  |  |  |  |  | 001111           |  |
| /dmul/o  | 10010000         | 10110110         |  |  |  |  |  | 00110001         |  |
| /dmul/c  | 1111000000000000 | 1111101001001010 |  |  |  |  |  | 0001001100111111 |  |
| /dmul/p  | 0000             | 1111             |  |  |  |  |  | 0101             |  |
| /dmul/g  | 0000             | 0000             |  |  |  |  |  | 0101             |  |
| /dmul/s  | 0100             | 0001             |  |  |  |  |  | 0100             |  |
| /dmul/m  | 1000             | 1110             |  |  |  |  |  | 0011             |  |
| /dmul/i  | 0                |                  |  |  |  |  |  |                  |  |

Fig. 7: Simulation results for Vedic multiplier Baugh – Wooley multiplier

The results of different implementation of Vedic multipliers are described. In Table IV. It is clear from the table, that the proposed multiplier is much more efficient than the earlier multiplier. The proposed architecture can be used to develop a low power with moderate delay Vedic multiplication using a Wallace tree multiplier.

Table III: Comparison of proposed Vedic multiplication with existing methods.

| Multipliers/<br>Parameters | Array Multiplier | Wallace Tree<br>Multiplier | Baugh-Wooley<br>Multiplier |
|----------------------------|------------------|----------------------------|----------------------------|
| Power                      | 5253.92          | 3792.22                    | 6799.87                    |
| Number of 4<br>input LUTs  | 6                | 6                          | 28                         |
| Number of<br>bonded IOBs   | 6                | 12                         | 22                         |
| Delay (ns)                 | 6.45             | 9.422                      | 14.365                     |
| No. of occupied<br>slices  | 3                | 6                          | 16                         |

## VI. CONCLUSION

Array multiplier, Wallace tree multiplier and Baugh Woolley multiplier has been synthesized on Xilinx Virtex-6 FPGA device. From the results, it can be concluded that the proposed architecture works more efficient than the other architecture proposed for Vedic multiplication. The array multiplier for Vedic multiplication gives a total delay of 6.45 ns which is less when compared to the total delay of any other multiplier. Similarly, the power consumption is low for the Vedic multiplication with the Wallace tree multiplier rather than the Baugh-Woolley multiplier. Compared with the Wallace tree multiplier, array multiplier which is used in existing method consumes high power of about 38.54%. The Baugh-Woolley multiplier also consumes of about 79.31% of more power than the Wallace tree multiplier.

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