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Comparative Study on Pipelined and Parallel Multiplier using Vedic Mathematics: A Review

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Abstract- Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). The design of high speed Vedic multiplier using the techniques of Vedic Mathematics that have been modified to improve performance A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. A typical processor devotes a considerable amount of processing time in performing arithmetic operations, particularly multiplication operations. Multiplication is one of the basic arithmetic operations and it requires substantially more hardware resources and processing time than addition and subtraction. Multiplication is a critical operation of Digital Signal processing (DSP) applications, Arithmetic and Logic Unit (ALU), multiply and Accumulated (MAC) unit. High Speed Multiplication is thus an essential requirement to increase the performance of processor. This paper reviews the design of a low power high speed algorithms for arithmetic logic units using this ancient mathematics techniques. The synthesized design using Xilinx ISE tool and Spartan3E.

Keywords*: **Vedic mathematics, ALU, multiply and Accumulated (MAC), igital Signal processing,*** graphics **processing units (GPUs), System-on-Chip (SoC).**

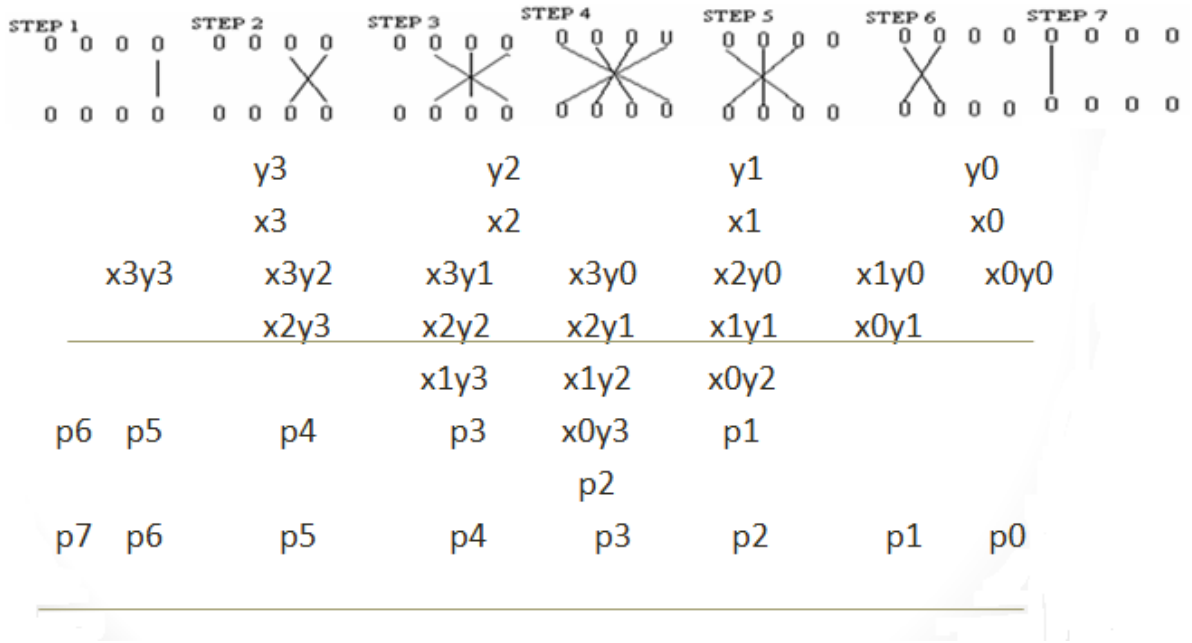
I. INTRODUCTION

In digital electronics, an arithmetic logic unit (*ALU*) is a digital circuit that performs integer arithmetic and logical operations. The ALU is a fundamental building block of the central processing unit of a computer, and even the simplest microprocessors contain one for purposes such as maintaining timers. The processors found inside modern CPUs and graphics processing units (GPUs) accommodate very powerful and very complex ALUs; a single component may contain a number of ALU. ALU is the important unit in Microprocessor/Microcontroller and CPU that performs Arithmetic operations like Addition, Subtraction, Multiplication and Division and Logical operations. Mostly in all of the ALU's the Logical operations are performed with the use of Pipelining and Parallel Processing Approach. And that's why the delay of the all the Logical operations is of only one gate Delay [1]. For example, if in the 32 bit ALU "and" operation is going to be performed then there will be the array of thirty-two and gates in parallel and the Ending operation will get performed in parallel way. So, there is not much Delay problem regarding the Logical Operations. But this problem is highly concerned with the Arithmetic Operations. And that's why we have designed a Delay optimized Arithmetic unit for the ALUs. Addition is a mathematical operation that represents the total number of objects together in a collection. Addition has several important properties. It is commutative, meaning that order does not matter, and it is associative, meaning that when one adds more than two numbers, the order in which addition is performed does not matter. Multiplication is one of the basic arithmetic operations and nearly 8.72 % of all the instruction in a typical processor is multiplication [2]. Multiplication process is used in many Neural computing and DSP applications like instrumentation and measurement, communications, audio and video processing, Graphics, image enhancement, 3-D rendering, Navigation, radar, GPS, and control applications like robotics, machine vision, guidance correlation etc. Most DSP tasks require real-time processing; it must perform these tasks speedily while minimizing Cost and Power. DIGITAL multipliers are the core components of all the digital signal processors (DSPs) and the speed of the DSP is largely determined by the speed of its multipliers. Also, the next generation of wireless network requires high-throughput and low power digital signal processing (DSP) System-on-Chip (SoC). Amongst the different building blocks of a DSP system, a multiplier is an essential component that has a significant role in both speed and power performance of the entire system. Therefore, to enhance the performance of DSP SoCs, designing of high performance and power efficient as well as delay efficient multiplier is crucial [3]. Since, multiplication dominates the execution

time of most DSP algorithms therefore high-speed multiplier is much desired. With an ever-increasing quest for greater computing power on battery-operated mobile devices, design emphasis has shifted from optimizing conventional delay time, area size to minimizing power dissipation while still maintaining the high performance. The low power and high speed multipliers can be implemented with different logic style.

II. RELATED WORK

Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in early twentieth century. Vedic mathematics is mainly based on sixteen principles or word formulae which are termed as Sutras. We discuss a possible application of Vedic mathematics to digital signal processing in the light of application of Vedic multiplication algorithm to digital multipliers. A simple digital multiplier (referred henceforth as Vedic multiplier) architecture based on the Urdhva Triyakbhyam (Vertically and Cross wise) Sutra is presented. This Sutra was traditionally used in ancient India for the multiplication of two decimal numbers in relatively less time. Ti was discovered for fast and convenient multiplication of decimal numbers. The biggest advantage is that, it can be implemented with reduces number of AND gates, FULL ADDERS and HALF ADDERS. Consider an example, which shows multiplication of decimal numbers, as shown in fig.



Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamhiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. The very word "Veda" has the derivational meaning i.e. the fountainhead and illimitable storehouse of all knowledge. Vedic mathematics is the name given to the ancient system of mathematics or, to be precise a unique technique of calculations based on simple rules and principles with which many mathematical problems can be solved, be it arithmetic, algebra, geometry or trigonometry. The system is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems.

Pipelining is one of the popular methods to realize high performance computing platform. Pipelining is a technique where multiple instruction executions are overlapped. It comes from the idea of a water pipe: continue sending water without waiting the water in the pipe to be out. By pipelining the unit of a system, we can produce result in every clock cycle. It leads to a reduction in the critical path. It can either increase the clock speed (or sampling speed) or reduces the power consumption at same speed in a DSP system.

III. LITERATURE REVIEW/SURVEY

In this paper, Ancient Indian system of mathematics known as Vedic mathematics can be applied to various branches of engineering to have a deeper insight into the working of various formulae. A typical processor devotes a considerable amount of processing time in performing arithmetic operations, particularly multiplication operation [4]. This paper presents the design of a low power high speed algorithm for arithmetic logic unit using this ancient mathematics technique also their hardware implementation. Employing this technique in the computation algorithm of the co-processor has reduced the complexity, execution time, area and power. The hardware can be implemented using Verilog HDL. In this paper, presenting a multiplier, in which the basic multiplication is perform using one of the technique of Vedic Mathematics and the accumulation of partial products is done using specific design. [5] In this technique intermediate product are generated in parallel that makes multiplication faster. Basic multiplier architecture is based on Vedic technique and accumulation is done using carry save adder, which gave better performance on comparison with other multiplier, that found the design works with much less delay. The synthesized design using Xilinx ISE tool and compared its speed with Modified Booth Wallace Multiplier and High speed Vedic Multiplier. The multiplier is implemented for low contrast image enhancement. This multiplier has been synthesizing on Spartan3E.The multipliers are the basic and essential building blocks of many high-performance systems. Multiplication is frequently used operation which is currently implemented in many processors. The word Vedic is deriving from the word Veda which means store house of all knowledge. Karatsuba of man is fast multiplication algorithm which helps to increase the speed of multiplier. Pipelined has long been known as efficient technique for optimizing the computational time. In this paper conclude that it gives comparison of clock frequency between pipeline and non-pipelined multiplier [6]. In this paper, improvement of speed over the conventional designs and then the result achieved by the proposed method has been compared by Karatsuba Multiplier. For the implementation of arithmetic unit using optimized Vedic multiplier which is not only useful for the optimizing the arithmetic unit of ALU but also is useful in the field of digital signal processing directly. The proposed arithmetic unit is coded in verilog HDL synthesized and simulated using Xilinx software. This paper presents study on high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like addition and shift. Further, the Verilog HDL coding of Urdhva tiryakbhyam Sutra. This paper presents the design of high speed Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance. A high-speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. This paper proposes a highly efficient method of multiplication – "Urdhva Tiryakbhyam Sutra" based on Vedic mathematics. It is a method for hierarchical multiplier design which clearly presents the computational advantages offered by Vedic methods. The computational path delay for proposed 8x8 bit Vedic multiplier is found to be 28.27 ns. It is observed that the Vedic multiplier is much more efficient than Array and Booth multiplier in terms of execution time [7]. for 8x8 bits multiplication and their FPGA implementation by Xilinx Synthesis Tool on Spartan 3 kit have been done and output has been displayed on LED's of Spartan 3 kit. The reason Behind choosing this yopic as a research work is that, ALU is the key element of digital processor like as microprocessor, microcontrollers, central processing unit etc. Every digital domain base technology depends upon the
operations performed by ALU either partially or whole, that's why it highly required designing high speed ALU, which can enhance the efficiency of those modules which lies upon the operations performed by ALU. The speed of ALU greatly depend upon the speed of multiplier. The conventional Vedic multiplication hardware's have some limitations. So, to overcome those limitations a novel approach has been proposed to design the Vedic multiplier with the use of unique addition tree structure, which used to add partially generated products. For designing the two bit Vedic multiplier conventional hardware of Vedic multiplier has been used. For designing the four and eight bit level
Vedic divide and conquer approach has been used. The proposed ALU is able to performed three different arithmetic and eight different logical operations at high speed. All of these operational sub-modules have been designed as the
combinatorial circuit and for synchronization, the multiplexers which have been used to integrate these sub-modules in a single unit have been triggered by positive edge clock. To design proposed arithmetic logic unit Verilog hardware
description language (HDL) has been used. For designing operational sub-modules data flow modelling and for integration purpose behavioral modelling style has been used. In which proposed a new technique to design Vedic multiplier using unique addition tree structure, which gives better response in terms of speed in comparison to the conventional Vedic multiplier [8].

IV. APPLICATIONS AND LIMITATION

With the explosive growth of VLSI system and portable devices, the power reduction of integrated circuits has become a major problem. In applications, such as communication system, cellular phone, camcorders and portable storage devices, low power dissipation, hence longer battery lifetime, is a must. To achieve a long-life operation of the portable device it is required to have a design system developed with faster operation and low power consumption. As most of the digital processing units are executed with mathematical operations, where a multiplier unit is dominantly being used, it is required to optimize a multiplier unit for overall system performance. Towards optimization of power consumption and speed improvement in [9] a digital level modeling of multiplier unit is proposed. The suggested parallel decimal multipliers are developed using VHDL definitions [10,11], and the power optimization [12] is observed to be evaluated for the seven mode of designing approaches in multiplier unit. Here, the design unit is developed in top down approach with delay and area coverage under consideration. The approach defines a relative energy consumption with respect to delay minimization in radix based multiplication operation [13,14]. Wherein delay is lower in radix operation, power consumption is observed to be high due to recurrent design approach. It is hence required to develop an equilibrium modeling in such design using delay power optimization. Towards the objective of achieving higher performance with low power consumption in [15,16, 17] bit level optimization is suggested. The coding efficiency in such coding is suggested via high level bit processing [18], suggested in ternary level operations. In the ternary level operation, the given bits are represented in 3 levels rather to 2 level representations as in binary mode. Due to 3 level representations, the processing speed of the system is observed to be higher, but the system overhead and area constraint are higher for such design. In recent approaches toward multiplier optimization, Vedic approach [19] of design modeling is emerging. This mode of design uses the concept of Vedic Math's to realize high level mathematical operation in a simpler modeling. Towards this approach in [20, 21] a high speed floating point operator using Vedic approach is suggested. The suggested multiplier unit, optimizes the usage based on successive adder and or units to achieve the results. In this approach, the speed of operation is observed to be higher, however, temporary buffering of the results bits is an overhead to this coding approach. There is a large register usage in such coding. The multiplier compiler design defined in [22] and [23] generate parameterizable layout for MOS technology, thus making them suitable for various high speed, low power, and compact VLSI implementations. However, area and speed are two important conflicting constraints. For real-time signal processing, a high speed and throughput Multipliers-Accumulator (MAC) is always a key to achieve high performance in the digital signal processing system. The main consideration of MAC design is to enhance its speeds. That high speed is achieved through this well-known Wallace tree multiplier [24,25]. Wallace introduced parallel multiplier architecture [26] to achieve high speed.

V. CONCLUSION

This paper outlines an extensive review on the developments made in the area of multiplier design. The applications of such multiplying unit in the real-time usage is presented. Resource optimization problem based on power consumption and hardware efficiency is observed. The upcoming approach of Vedic algorithm in usage of arithmetic
operation and its usage in multiplier design is presented. The limitation in regards to these conventional design approach is addressed. The above result shown in table, are studied from referred literature. As compared to above result, in future the proposed work presented in this paper will give better result in terms of mention parameter by using concept of pipelining in Vedic multiplier for ALU.

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